Application Note

AN_209

AN_209 PDIUSBD12 to FT120 Migration Guide

Version 1.1

Issue Date: 2012-12-14

The FT120 is a cost and feature optimized USB Full-Speed device controller. It communicates with a micro-controller over a generic parallel interface, and integrates USB device/slave functionality into a system. This application note describes how to implement the device in legacy designs where the PDIUSBD12 was being used, as well as some minor differences between the two chips.

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1 Introduction

The FT120 is a cost and feature optimized USB full-speed device controller. It communicates with a micro-controller over the generic parallel interface. The design closely matches the PDIUSBD12 which has been a very popular USB solution over the past decade, but is now becoming increasingly difficult to source in volume. To fill this gap in the market, the FT120T (28 pin TSSOP package) may be used in designs originally intended for PDIUSBD12 devices by following the advice in this application note.

2 FT120 vs PDIUSBD12

2.1 Features

The main features of the two generations of devices are shown below. To maximize compatibility, the 28 pin TSSOP package has been selected.

FEATURE	FT120	PDIUSBD12
MECHANICAL		
Packages	28 pin TSSOP 28 Pin QFN	28 pin TSSOP SO28
Temperature	-40°C to 85°C	-40°C to 85°C
ELECTRICAL		
VCC Supply	3V3 or 5.0V	3V3 or 5.0V
IO Levels	3V3 (5V tolerant)	3V3 or 5.0V
Operating Current	7mA	15mA
Suspend current	83uA	15uA
USB Modes		
Speed	Full Speed	Full Speed
Transfer Modes	Bulk / Isochronous / Interrupt	Bulk / Isochronous / Interrupt
DATA THROUGHPUT		
Bulk mode	Up to 1MByte/s (typical)	Up to 1MByte/s (typical)
Isochronous mode	Up to 1Mbit/s (typical)	Up to 1Mbit/s (typical)
DMA ENGINE	YES	YES

Table 2.1 Feature comparison

2.2 Pinout

The pinout of the two devices match as per the table below:

PIN	FT120T	PDIUSBD12	DESCRIPTION
1	DATA0	DATA0	Bit 0 of bi-directional data.
2	DATA1	DATA1	Bit 1 of bi-directional data.
3	DATA2	DATA2	Bit 2 of bi-directional data.
4	DATA3	DATA3	Bit 3 of bi-directional data.
5	GND	GND	Ground
6	DATA4	DATA4	Bit 4 of bi-directional data.
7	DATA5	DATA5	Bit 5 of bi-directional data.
8	DATA6	DATA6	Bit 6 of bi-directional data.
9	DATA7	DATA7	Bit 7 of bi-directional data.
10	ALE	ALE	Address Latch Enable. The falling edge is used to close the latch of the address information in a multiplexed address/ data bus. Permanently tied low for separate address/ data bus configuration.
11	CS_N	CS_N	Chip Select (Active Low)
12	SUSPEND	SUSPEND	Device suspend(output) and wakeup(input)
13	CLKOUT	CLKOUT	Programmable Output Clock
14	INT_N	INT_N	Interrupt (Active Low)
15	RD_N	RD_N	Read Strobe (Active Low)
16	WR_N	WR_N	Write Strobe (Active Low)
17	DMREQ	DMREQ	DMA Request.
18	DMACK_N	DMACK_N	DMA Acknowledge (Active Low).
19	EOT_N	EOT_N	End of DMA Transfer (Active Low). Double up as Vbus sensing. EOT_N is only valid when asserted together with DMACK_N and either RD_N or WR_N.
20	RESET_N	RESET_N	Reset (Active Low and asynchronous). Built-in power-on reset circuit is present on-chip, so this pin can be tied to VCC.

PIN	FT120T	PDIUSBD12	DESCRIPTION
21	GL_N	GL_N	USB traffic LED indicator (Active Low)
22	XTAL1	XTAL1	Crystal connection 1 (6MHz); alternatively, a 1.8V square wave clock can be applied.
23	XTAL2	XTAL2	Crystal connection 2 (6MHz) ; if the external clock signal, instead of the crystal, is connected to XTAL1, then XTAL2 should be left unconnected
24	Vcc	Vcc	Voltage supply (4.0 - 5.5V); To operate the IC at 3.3 V, supply 3.3 V to both the VCC and 3V3OUT pins
25	USBDM	D-	USB D- data line
26	USBDP	D+	USB D+ data line
27	3V3OUT	VOUT3.3	3.3V regulated output; To operate the IC at 3.3 V, supply 3.3 V to both the VCC and 3V3OUT pins
28	A0	A0	Address bit. A0=1 selects command instruction; A0=0 selects the data phase. This pin is ignored in the multiplexed address and data bus configuration and should be tied to HIGH.

Table 2.2 Pinout comparison

3 Reference Schematic

Figure 3.1 shows a reference schematic. All power and termination options are the same as per a PDIUSBD12 schematic.

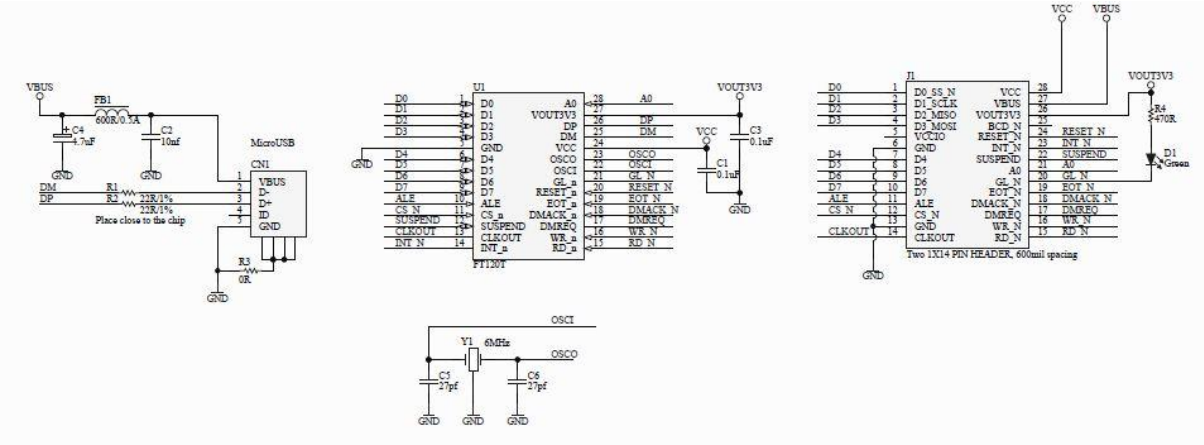

Figure 3.1 Reference Schematic

4 BOM Changes Required

The only BOM change required to a design already using a PDIUSBD12 28 pin TSSOP device is to replace the device with the FT120.

5 Firmware

The register map for the PDIUSBD12 and the FT120 are the same. This allows the control firmware used for the PDIUSBD12 to be compatible with the FT120 and therefore application software should not need to be changed. FTDI recommends that application software be revalidated with the new chip.

Command Name	Recipient	Coding	Data phase
Initialization Commands			
Set Address / Enable	Device	D0h	Write 1 byte
Set Endpoint Enable	Device	D8h	Write 1 byte
Set Mode	Device	F3h	Write 2 byte
Set DMA	Device	FBh	Write/Read 1 byte
Data Flow Commands			
Read Interrupt Register	Device	F4h	Read 2 bytes
Select Endpoint	Control OUT	00h	Read 1 byte (optional)
	Control IN	01h	Read 1 byte (optional)
	Endpoint 1 OUT	02h	Read 1 byte (optional)
	Endpoint 1 IN	03h	Read 1 byte (optional)
	Endpoint 2 OUT	04h	Read 1 byte (optional)
	Endpoint 2 IN	05h	Read 1 byte (optional)
Read Last Transaction Status	Control OUT	40h	Read 1 byte
	Control IN	41h	Read 1 byte
	Endpoint 1 OUT	42h	Read 1 byte
	Endpoint 1 IN	43h	Read 1 byte
	Endpoint 2 OUT	44h	Read 1 byte
	Endpoint 2 IN	45h	Read 1 byte
Read Endpoint Status	Control OUT	80h	Read 1 byte
	Control IN	81h	Read 1 byte
	Endpoint 1 OUT	82h	Read 1 byte
	Endpoint 1 IN	83h	Read 1 byte
	Endpoint 2 OUT	84h	Read 1 byte

	Endpoint 2 IN	85h	Read 1 byte
Read Buffer	Selected Endpoint	F0h	Read n bytes
Write Buffer	Selected Endpoint	F0h	Write n bytes
Set Endpoint Status	Control OUT	40h	Write 1 byte
	Control IN	41h	Write 1 byte
	Endpoint 1 OUT	42h	Write 1 byte
	Endpoint 1 IN	43h	Write 1 byte
	Endpoint 2 OUT	44h	Write 1 byte
	Endpoint 2 IN	45h	Write 1 byte
Acknowledge Setup	Selected Endpoint	F1h	None
Clear Buffer	Selected Endpoint	F2h	None
Validate Buffer	Selected Endpoint	FAh	None
General Commands			
Send Resume		F6h	None
Read Current Frame Number		F5h	Read 1 or 2 bytes

Table 5.1 Register list

The bit mapping for each register is available in the FT120 datasheet.

5.1 Set DMA Functional Difference

In register FB (Set DMA) bits 6 and 7 allow for interrupts to be enabled / disabled.

With the PDIUSBD12, interrupts will be generated regardless of the setting in this register.

With the FT120, the interrupt will be enabled/disabled according to the value set when used in DMA mode.

To ensure maximum compatibility with PDIUSBD12 designs it is recommended the interrupts are enabled in this register. However new designs may use these bits to set the interrupts as per the design requirements.

Firmware using non-DMA mode is not affected.

5.2 CLKOUT and SUSPEND Pin Differences

The FT120 has a variety of different clock modes configured with the Set Mode register F3 as shown in Table 5.2 affecting the CLKOUT and SUSPEND pin.

Mode	Configuration bits		CLKOUT output (errata 3.1.3)			SUSPEND output (errata 3.1.2)			existing suspend handler	Recommended Workaround
			normal operation	suspend mode		normal operation	suspend mode			
	NO LAZY CLOCK	CLOCK RUNNING		D12	FT120		D12	FT120		
0	0	0	Divided Clock	Lazy Clock	Lazy Clock	LOW	HIGH	HIGH	pin	Not required
1	0	1	Divided Clock	Lazy Clock	Divided Clock	LOW	HIGH	LOW	interrupt	Firmware change to mode 0, change to handle suspend by pin
									pin	FW change to mode 0
2	1	0	Divided Clock	No Clock	No Clock	LOW	HIGH	HIGH	pin	Not required
3	1	1	Divided Clock	Divided Clock	Divided Clock	LOW	HIGH	LOW	interrupt	Not required
									pin	Firmware change to handle suspend by interrupt

Table 5.2 Clock Modes

Modes 0 and 3 are 100% backward compatible with the PDIUSBD12, but for designs originally using mode 1, (NO LAZY CLOCK = 0 and CLOCK RUNNING = 1) it is recommended to alter the firmware to use mode 0. Thus ensuring the CLKOUT pin "Lazy clock" is enabled and the SUSPEND pin is logic 1 during suspend mode.

For designs originally using mode 3, (NO LAZY CLOCK =1 and CLOCK RUNNNIG = 1) the SUSPEND pin will not drive high as per USBD12 designs.

Firmware can be modified to set the CLOCK RUNNING bit of Set Mode command to be '0' (Mode 0 or Mode 2). Under this configuration the CLKOUT will switch to 30 kHz suspend clock upon entering USB suspend state. To resume the USB bus, firmware needs to wakeup FT120 by drive the SUSPEND pin to LOW, and then issue Send Resume command to FT120.

6 IO Levels

The FT120 has been designed to be used in 3V3 systems. The IO pins are designed to drive out at 3V3 levels, but support input levels from 3V3 to 5V.

In many systems 3V3 output will be sufficient to drive 5V logic, but in other cases it may require additional logic to boost the logic level.

The PDIUSBD12 device was designed to operate in 3V3 to 5V systems and as such is capable of driving out at 3V3 to 5V levels.

7 Ordering Information.

Part Number	Package
FT120T-00-U	28 Pin TSSOP, Tube

Table 7.1 Part numbers

8 Summary

Updating an existing design from a PDIUSBD12 to the FT120 should be a simple process, requiring a small BOM change ie swap the PDIUSBD12 out for the FT120T. All existing and proven firmware shall run on the new FT120T as it did on the original device. This solution allows for a rapid upgrade to ensure designs which may have been deemed obsolete due to supply difficulties with the original parts can enjoy an extended life span.

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Appendix A – References

Document References

FT120 Data Sheet

Acronyms and Abbreviations

Terms	Description
DMA	Direct Memory Access
USB	Universal Serial Bus

Appendix B – List of Tables & Figures

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Appendix C – Revision History

Document Title: AN_209 PDIUSBD12 to FT120 Migration Guide
Document Reference No.: FT_000676
Clearance No.: FTDI# 289
Product Page: http://www.ftdichip.com/FTProducts.htm
Document Feedback: Send Feedback

Revision	Changes	Date
1.0	Initial Release	2012-M05-08
1.1	Added section 6 on IO levels Update contact info	2012-12-14