Future Technology Devices International Ltd.

Application Note AN_150

A Comparison between MORPHIC-1K and Morph-IC-II FPGA Development Modules

Document Reference No.: FT_000303

Version 1.0

Issue Date: 2010-08-20

This application note describes the differences between the FTDI MorphIC-1K and MORPH-IC-II. Sub-100ms FPGA programming/re-programming makes Morph-IC-II ideal for applications which require users to reconfigure hardware functionality 'on-the-fly' by downloading new software over USB : "morphing" the hardware.

Future Technology Devices International Limited (FTDI)

Unit 1, 2 Seaward Place, Glasgow G41 1HH, United Kingdom
Tel.: +44 (0) 141 429 2777 Fax: + 44 (0) 141 429 2758
E-Mail (Support): **support1@ftdichip.com** Web: http://www.ftdichip.com

Table of Contents

1 Introduction

FTDI have taken the existing FTDI MorphIC-1K FPGA development module, enhanced it and increased its capabilities, flexibility and power. The enhanced MorphIC is called "Morph-IC-II". Sub-100ms FPGA programming/re-programming makes Morph-IC-II ideal for applications which require users to reconfigure hardware functionality 'on-the-fly' by downloading new software over USB : "morphing" the hardware.

The following chapters give a brief overview of the enhancements.

2 Morph-IC-II Enhancements

The enhanced features of Morph-IC-II are as follows:

- Morph-IC-II has up to 80 I/Os whereas the MorphIC-1K had only 40 I/Os, these I/Os were introduced by extending the length of the module by 32mm.
- Morph-IC-II uses a Hi-Speed USB 2.0 interface whereas MorphIC-1K used a Full-Speed USB 2.0 interface.
- Morph-IC-II uses an EP2C5F256C8N which has 4,608 Logic Elements where MorphIC-1K used a EP1K10TC100-3 which has only 576 Logic Elements.
- Morph-IC-II has the ability to be programmed using JTAG programming interface. This was not available on MorphIC-1K.
- Morph-IC-II can use either a Synchronous or an Asynchronous 245 FIFO interfaces to communicate between the USB interface bridge and the FPGA. Synchronous 245 FIFO can transfer data at higher rates than Asynchronous 245 FIFO. MorphIC-1K only had an Asynchronous 245 FIFO interfaces.
- Morph-IC-II has six GPIO port connections available. These connections are between the USB bridge and the FPGA. These lines were not available on MorphIC-1K. These lines can be used in applications such as controlling chip select lines or setting a status line which can be connected to a LED.
- Morph-IC-II can operate using signals that have different *logic voltage levels*. This was not available on MorphIC-1K.

These enhancements are summarised in Table 1.

MorphIC-1K	Morph-IC-II
40 I/Os	80 I/Os
Full-Speed USB 2.0	Hi-Speed USB 2.0
EP1K10TC100-3 FPGA which has 576 Logic Elements	EP2C5F256C8N FPGA which has 4,608 Logic Elements
No JTAG programming interface that is SignalTap compatible	JTAG programming interface that is SignalTap compatible
Asynchronous 245 FIFO	Synchronous or an Asynchronous 245 FIFO
No GPIO port connections available	Has six GPIO port connections available
All I/Os fixed to 3.3V TTL/CMOS	Morph-IC-II can operate using signals that have different *logic voltage levels*. This was not available on MorphIC-1K

Table 1 - A Comparison between the two MorphIC modules

This application note describes the enhancements made while developing Morph-IC-II and describes the effects of these changes may have on MorphIC-1K designs.

2.1 Scope

The most obvious difference between MorphIC-1K and Morph-IC-II modules is the physical size. Morph-IC-II is much longer than MorphIC-1K. This provides an additional 40 I/Os which gives greater flexibility in the development of many applications based on Morph-IC-II.

The change in size does not affect backward compatibility. Existing MorphIC-1K designs can still use Morph-IC-II module. MorphIC-1K I/Os are on similar connector pins as Morph-IC-II. The additional IO are routed to 2 additional connectors.

Every signal assigned to J1 and J2 headers on Morph-IC-II operate in the same way as in MorphIC-1K with the exception that some I/Os on the Morph-IC-II can operate at different voltage levels (depending on the position of the onboard jumper V_BANK4).

The I/Os connected to I/O Bank4 of Morph-IC-II's FPGA are capable of transferring signals that have a *logic voltage level* other than 3.3 volts. The I/Os connected to the other I/O Banks of Morph-IC-II's FPGA can only process signals of 3.3 volts. When the Jumper "V_Bank 4" is closed I/O Bank4 is configured to interface to signals of 3.3 volts which is the same as MorphIC-1K. If this jumper is removed, the signal levels of I/O Bank4 are determined by an externally supplied voltage.

Data communications between the Altera FPGA on Morph-IC-II and FTDI USB FT2232H Bridge chip differs in the two modules. MorphIC-1K uses channel B of the FT2232D to transfer the data over a parallel 245 FIFO interface, while Morph-IC-II uses channel A of the FT2232H to transfer the data over this parallel 245 FIFO interface. This change was introduced to facilitate the option of using a synchronous 245 FIFO interface. This change needs to be noted when running MorphIC-1K applications on Morph-IC-II.

3 MorphIC-1K and Morph-IC-II Pin-Out

The following diagrams, Figure 1 and Figure 2, compare the pin out of Morph-IC-II and MorphIC-1K modules. These diagrams indicate that J1 and J2 are similar for both modules – with the exception of the signal V_BANK4 on J2 which will supply the voltage level for BANK4 of the FPGA when the V-BANK4 link is removed on the Morph-IC-II module.

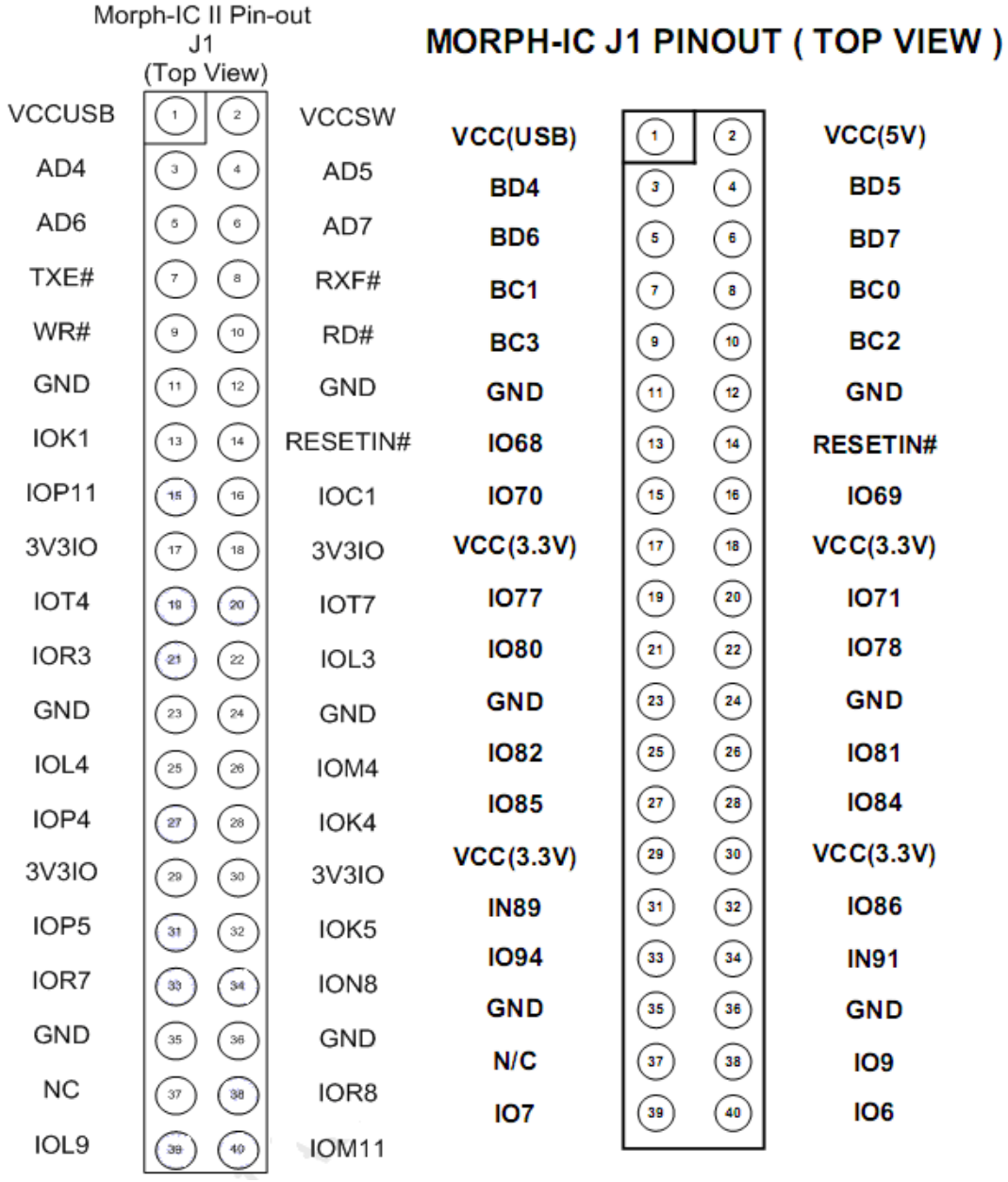

Fig. 1 – A comparison of J1 between the Morph-IC and the Morph-IC-II

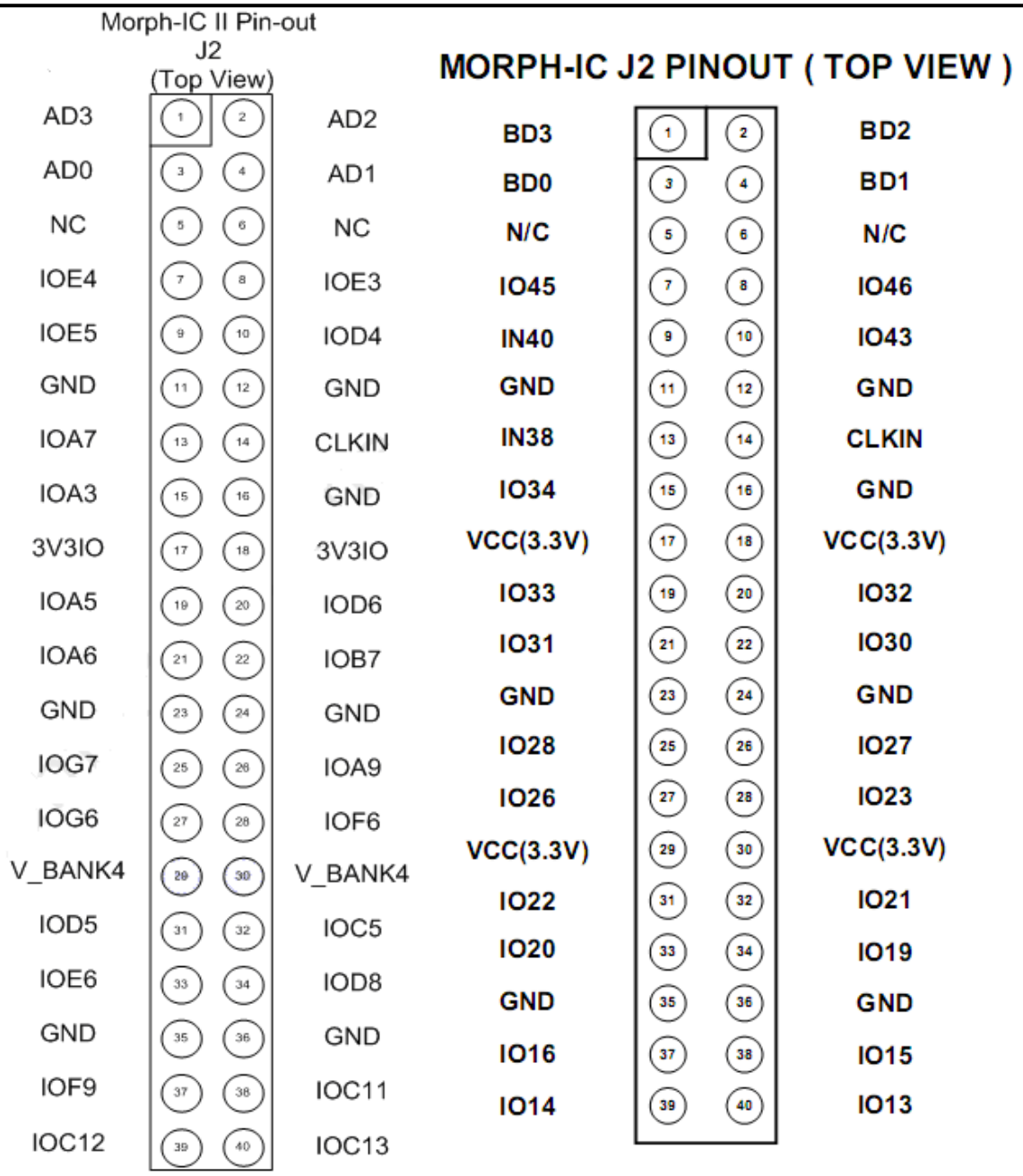

Fig. 2 – A comparison of J2 between the MorphIC-1K and the Morph-IC-II

4 MorphIC-1K and Morph-IC-II Mechanical Details

The mechanical Details of Morph-IC-II are given in Fig. 3 and the mechanical details for MorphIC-1K are given in Fig. 4. It can be calculated from comparing these two figures that the length of Morph-IC-II is approximately 32mm longer. The distance between the headers of both modules is the same which will allow for backward compatibility.

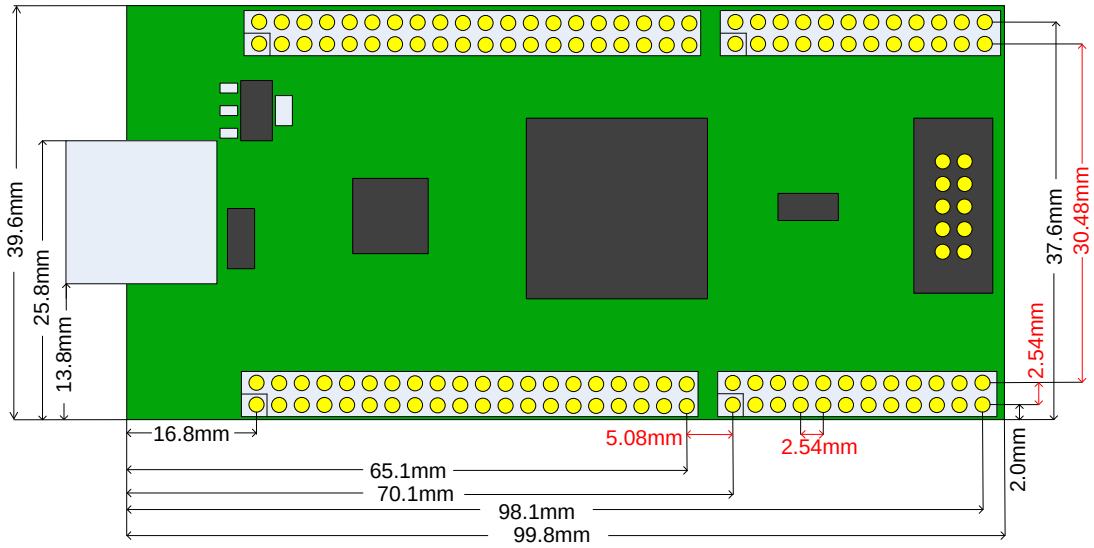

Fig. 3 – Morph-IC-II Mechanical Details

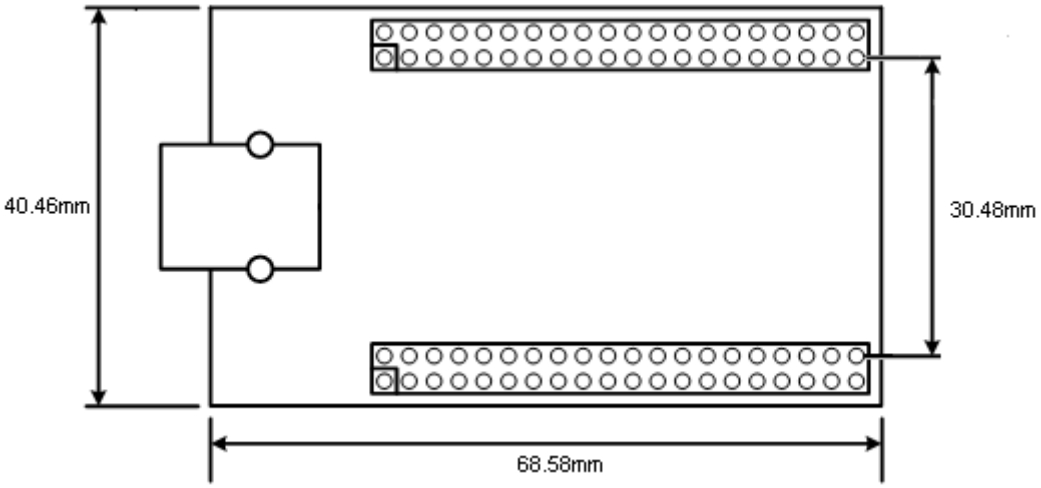

Fig. 4 – MorphIC-1K Mechanical Details

5 Contact Information

Head Office – Glasgow, UK

Future Technology Devices International Limited
Unit 1, 2 Seaward Place, Centurion Business Park
Glasgow G41 1HH
United Kingdom
Tel: +44 (0) 141 429 2777
Fax: +44 (0) 141 429 2758

E-mail (Sales) sales1@ftdichip.com
E-mail (Support) support1@ftdichip.com
E-mail (General Enquiries) admin1@ftdichip.com
Web Site URL http://www.ftdichip.com
Web Shop URL http://www.ftdichip.com

Branch Office – Taipei, Taiwan

Future Technology Devices International Limited (Taiwan)
2F, No. 516, Sec. 1, NeiHu Road
Taipei 114
Taiwan , R.O.C.
Tel: +886 (0) 2 8791 3570
Fax: +886 (0) 2 8791 3576

E-mail (Sales) tw.sales1@ftdichip.com
E-mail (Support) tw.support1@ftdichip.com
E-mail (General Enquiries) tw.admin1@ftdichip.com
Web Site URL http://www.ftdichip.com

Branch Office – Hillsboro, Oregon, USA

Future Technology Devices International Limited (USA)
7235 NW Evergreen Parkway, Suite 600
Hillsboro, OR 97123-5803
USA
Tel: +1 (503) 547 0988
Fax: +1 (503) 547 0987

E-Mail (Sales) us.sales@ftdichip.com
E-Mail (Support) us.support@ftdichip.com
E-Mail (General Enquiries) us.admin@ftdichip.com
Web Site URL http://www.ftdichip.com

Branch Office – Shanghai, China

Future Technology Devices International Limited (China)
Room 408, 317 Xianxia Road,
Shanghai, 200051
China
Tel: +86 21 62351596
Fax: +86 21 62351595

E-mail (Sales) cn.sales@ftdichip.com
E-mail (Support) cn.support@ftdichip.com
E-mail (General Enquiries) cn.admin@ftdichip.com
Web Site URL http://www.ftdichip.com

Distributor and Sales Representatives

Please visit the Sales Network page of the FTDI Web site for the contact details of our distributor(s) and sales representative(s) in your country.

6 Appendix A – References

Document References

DS_Morph-IC-II

AN_141_MorphIO-II and MorphLd Utilities for Morph-IC-II

www.ftdichip.com

Acronyms and Abbreviations

Terms	Description
FIFO	First In First Out serial interface
FPGA	Field Programmable Gate Array
USB	Universal Serial Bus
GPIO	General Purpose Input Output
JTAG	Joint Test Action Group

7 Appendix B – Revision History

Revision	Changes	Date
1.0	Initial Release	13th August 2010