



FTDI Future Technology Devices International

Application Note

AN_184

FTDI Device Input Output pin States

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This application note describes the reset, suspend and active states of the input / output pins of the following devices: FT232R, FT245R, FT232H, FT2232H, FT4232H & FT2232D.

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1 Introduction

This application note explains the various states of input and output pins of the following FTDI devices: FT232R, FT245R, FT232H, FT2232H, FT4232H & FT2232D.

Note: The convention used throughout this document for active low signals is the signal name followed by a #.

1.1 Applicable Documents

The following data sheets can be downloaded by clicking on the appropriate links below:

[FT232R USB UART IC Data Sheet](#)

[FT245R USB FIFO Data Sheet](#)

[FT232H Single Channel Hi-Speed USB to Multipurpose UART/FIFO IC](#)

[FT2232H Hi-Speed Dual USB UART/FIFO IC Data Sheet](#)

[FT4232H Hi-Speed Quad USB UART IC Data Sheet](#)

[FT2232D Dual USB UART/FIFO IC Data Sheet](#)

2 FT232R – I/O Pins

FT232R						
Pin Name	Pin Number	RESET# Low	SUSPEND (Pull Down IO Pins in USB Suspend - Not Set)	SUSPEND (Pull Down IO Pins in USB Suspend - Set)	During Enumeration (out of reset prior to EEPROM read)	Active (device enumerated after eeprom read)
CBUS 0	23	TriSt- PU	Selected Function	TriSt-PD	Driving Low	Selected Function
CBUS 1	22	TriSt- PU	Selected Function	TriSt-PD	Driving Low	Selected Function
CBUS 2	13	TriSt- PU	Selected Function	TriSt-PD	Driving Low	Selected Function
CBUS 3	14	TriSt	Selected Function	TriSt-PD	Input	Selected Function
CBUS 4	12	TriSt	Selected Function	TriSt-PD	Input	Selected Function
TXD	1	TriSt- PU	Output	TriSt-PD	TriSt- PU	Output
DTR#	2	TriSt- PU	Output	TriSt-PD	TriSt- PU	Output
RTS#	3	TriSt- PU	Output	TriSt-PD	TriSt- PU	Output
RXD	5	TriSt- PU	TriSt- PU	TriSt-PD	TriSt- PU	TriSt- PU
RI#	6	TriSt- PU	TriSt- PU	TriSt-PD	TriSt- PU	TriSt- PU
DSR#	9	TriSt- PU	TriSt- PU	TriSt-PD	TriSt- PU	TriSt- PU
DCD#	10	TriSt- PU	TriSt- PU	TriSt-PD	TriSt- PU	TriSt- PU
CTS#	11	TriSt- PU	TriSt- PU	TriSt-PD	TriSt- PU	TriSt- PU

Table 2.1 FT232R I/O States

2.1 FT232R - CBUS Selected Function

FT232R													
Pin	TXD N	PWRO N#	RXLE D#	TXLE D#	TX & RXLE D#	SLEEP#	CLK 48	CLK 24	CLK 12	CLK 6	I/O Mode	BitBanging WRn	BitBanging RDn
CBUS 0	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
CBUS 1	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
CBUS 2	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
CBUS 3	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
CBUS 4	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	x	x	x

Table 2.2 FT232R CBUS selected functions

3 FT245R - I/O Pins

FT245R						
Pin Name	Pin Number	RESET# Low	SUSPENDED (Pull Down IO Pins in USB Suspend - Not Set)	SUSPEND (Pull Down IO Pins in USB Suspend - Set)	During Enumeration (out of reset prior to EEPROM read)	Active (device enumerated after eeprom read)
RXF#	23	TriSt- PU	RXF#	TriSt-PD	Driving Low	Output
TXE#	22	TriSt- PU	TXE#	TriSt-PD	Driving Low	Output
RD#	13	TriSt- PU	RD#	TriSt-PD	Driving Low	Input
WR	14	TriSt	WR#	TriSt-PD	Input	Input
PWREN#	12	TriSt	PWREN#	TriSt-PD	Input	PWREN#
D0	1	TriSt- PU	TriSt- PU driving when RD# is low	TriSt-PD	TriSt- PU	TriSt- PU driving when RD# is low
D1	5	TriSt- PU	TriSt- PU driving when RD# is low	TriSt-PD	TriSt- PU	TriSt- PU driving when RD# is low
D2	3	TriSt- PU	TriSt- PU driving when RD# is low	TriSt-PD	TriSt- PU	TriSt- PU driving when RD# is low
D3	11	TriSt- PU	TriSt- PU driving when RD# is low	TriSt-PD	TriSt- PU	TriSt- PU driving when RD# is low
D4	2	TriSt- PU	TriSt- PU driving when RD# is low	TriSt-PD	TriSt- PU	TriSt- PU driving when RD# is low
D5	9	TriSt- PU	TriSt- PU driving when RD# is low	TriSt-PD	TriSt- PU	TriSt- PU driving when RD# is low
D6	10	TriSt- PU	TriSt- PU driving when RD# is low	TriSt-PD	TriSt- PU	TriSt- PU driving when RD# is low
D7	6	TriSt- PU	TriSt- PU driving when RD# is low	TriSt-PD	TriSt- PU	TriSt- PU driving when RD# is low

Table 3.1 FT245R I/O States

4 FT232H– I/O Pins

FT232H							
Pin Name	Pin Number	RESET# Low	Default	SUSPEND (Pull Down IO Pins in USB Suspend - Not Set)	SUSPEND (Pull Down IO Pins in USB Suspend - Set)	During Enumeration (out of reset prior to EEPROM read)	Active (device enumerated after eeprom read)
ADBUS0	13	Input	TXD	Function	TriSt-PD	Output	Function
ADBUS1	14	Input-PU	RXD	Function	TriSt-PD	Input-PU	Function
ADBUS2	15	Input	RTS#	Function	TriSt-PD	Output	Function
ADBUS3	16	Input-PU	CTS#	Function	TriSt-PD	Input-PU	Function
ADBUS4	17	Input	DTR#	Function	TriSt-PD	Output	Function
ADBUS5	18	Input-PU	DSR#	Function	TriSt-PD	Input-PU	Function
ADBUS6	19	Input-PU	DCD#	Function	TriSt-PD	Input-PU	Function
ADBUS7	20	Input-PU	RI#	Function	TriSt-PD	Input-PU	Function
ACBUS0	21	TriSt-PU	TriSt-PU	Function/Selecti on	TriSt-PD	TriSt-PU	Function/Select ion
ACBUS1	25	TriSt-PU	TriSt-PU	Function/Selecti on	TriSt-PD	TriSt-PU	Function/Select ion
ACBUS2	26	TriSt-PU	TriSt-PU	Function/Selecti on	TriSt-PD	TriSt-PU	Function/Select ion
ACBUS3	27	TriSt-PU	TriSt-PU	Function/Selecti on	TriSt-PD	TriSt-PU	Function/Select ion
ACBUS4	28	TriSt-PU	TriSt-PU	Function/Selecti on	TriSt-PD	TriSt-PU	Function/Select ion
ACBUS5	29	TriSt-PU	TriSt-PU	Function/Selecti on	TriSt-PD	TriSt-PU	Function/Select ion
ACBUS6	30	TriSt-PU	TriSt-PU	Function/Selecti on	TriSt-PD	TriSt-PU	Function/Select ion
ACBUS7	31	TriSt-PD	TriSt-PU	Input-PD or MPSSE	TriSt-PD	TriSt-PD	Input-PD or MPSSE
ACBUS8	32	TriSt-PU	TriSt-PU	Function/Selecti on	TriSt-PD	TriSt-PU	Function/Select ion
ACBUS9	33	TriSt-PU	TriSt-PU	Function/Selecti on	TriSt-PD	TriSt-PU	Function/Select ion

Table 4.1 FT232H I/O States

4.1 FT232H - Selected Function

FT232H										
Pin		Pin functions (depends on configuration)								
Pin #	Pin Name	ASYNC Serial RS232	245 FIFO SYNC	245 FIFO	ASYNC Bit-bang	SYNC Bit-bang	MPSSE	Fast Serial interface	CPU Style FIFO	FT1248
13	ADBUS0	TXD	D0	D0	D0	D0	TCK/SK	FSDI	D0	MIOSI0
14	ADBUS1	RXD	D1	D1	D1	D1	TDI/DO	FSCLK	D1	MIOSI1
15	ADBUS2	RTS#	D2	D2	D2	D2	TDO/DI	FSDO	D2	MIOSI2
16	ADBUS3	CTS#	D3	D3	D3	D3	TMS/CS	FSCTS	D3	MIOSI3
17	ADBUS4	DTR#	D4	D4	D4	D4	GPIOL0	** TriSt-UP	D4	MIOSI4
18	ADBUS5	DSR#	D5	D5	D5	D5	GPIOL1	** TriSt-UP	D5	MIOSI5
19	ADBUS6	DCD#	D6	D6	D6	D6	GPIOL2	** TriSt-UP	D6	MIOSI6
20	ADBUS7	RI#	D7	D7	D7	D7	GPIOL3	** TriSt-UP	D7	MIOSI7
21	ACBUS0	* TXDEN	RXF#	RXF#	ACBUS0	ACBUS0	GPIOH0	** ACBUS0	CS#	SCLK
25	ACBUS1	** ACBUS 1	TXE#	TXE#	WRSTB#	WRSTB#	GPIOH1	** ACBUS1	A0	SS_N
26	ACBUS2	** ACBUS 2	RD#	RD#	RDSTB#	RDSTB#	GPIOH2	** ACBUS2	RD#	MISO
27	ACBUS3	* RXLED #	WR	WR	ACBUS3	ACBUS3	GPIOH3	** ACBUS3	WR	ACBUS3
28	ACBUS4	* TXLED #	SIWU#	SIWU#	SIWU#	SIWU#	GPIOH4	SIWU#	SIWU#	ACBUS4
29	ACBUS5	** ACBUS 5	CLKOUT	ACBUS5	** ACBUS5	** ACBUS5	GPIOH5	** ACBUS5	** ACBUS5	ACBUS5
30	ACBUS6	** ACBUS 6	OE#	ACBUS6	ACBUS6	ACBUS6	GPIOH6	** ACBUS6	** ACBUS6	ACBUS6
31	ACBUS7	** USBVC C	USBVCC	USBVCC	USBVCC	USBVCC	GPIOH7	USBVCC	USBVCC	USBVCC
32	ACBUS8	** ACBUS 8	** ACBUS8	** ACBUS8	** ACBUS8	** ACBUS8	** ACBUS8	** ACBUS8	** ACBUS8	ACBUS8
33	ACBUS9	** ACBUS 9	** ACBUS9	** ACBUS9	** ACBUS9	** ACBUS9	** ACBUS9	** ACBUS9	** ACBUS9	ACBUS9

Table 4.2 FT232H Selected functions

Pins marked * are EEPROM selectable.

Pins marked ** default to tri-stated inputs with an internal 75K Ω (approx) pull up resistor to VCCIO.

Pin marked *** default to GPIO line with an internal 75K Ω pull down resistor to GND. Using the EEPROM this pin can be enabled USBVCC mode instead of GPIO mode.

5 FT2232H – Channel A Pins

FT2232H Channel A							
Pin Name	Pin Number	RESET# Low	Default	SUSPEND (Pull Down IO Pins in Suspend - Not Set)	SUSPEND (Pull Down IO Pins in USB Suspend - Set)	During Enumeration (out of reset prior to EEPROM read)	Active (device enumerated after eeprom read)
16	ADBUS0	TriSt	TXD	Function	TriSt-PD	TXD	Function
17	ADBUS1	TriSt-PU	RXD	Function	TriSt-PD	RXD	Function
18	ADBUS2	TriSt	RTS#	Function	TriSt-PD	RTS#	Function
19	ADBUS3	TriSt-PU	CTS#	Function	TriSt-PD	CTS#	Function
21	ADBUS4	TriSt	DTR#	Function	TriSt-PD	DTR#	Function
22	ADBUS5	TriSt-PU	DSR#	Function	TriSt-PD	DSR#	Function
23	ADBUS6	TriSt-PU	DCD#	Function	TriSt-PD	DCD#	Function
24	ADBUS7	TriSt-PU	RI#	Function	TriSt-PD	RI#	Function
26	ACBUS0	TriSt	TXDEN	Function	TriSt-PD	TXDEN	Function
27	ACBUS1	TriSt-PU	TriSt-PU	Function	TriSt-PD	TriSt-PU	Function
28	ACBUS2	TriSt-PU	TriSt-PU	Function	TriSt-PD	TriSt-PU	Function
29	ACBUS3	TriSt-PU	RXLED#	Function	TriSt-PD	TriSt-PU	Function
30	ACBUS4	TriSt-PU	TXLED#	Function	TriSt-PD	TriSt-PU	Function
32	ACBUS5	TriSt-PU	TriSt-PU	Function	TriSt-PD	TriSt-PU	Function
33	ACBUS6	TriSt-PU	TriSt-PU	Function	TriSt-PD	TriSt-PU	Function
34	ACBUS7	TriSt-PU	TriSt-PU	Function	TriSt-PD	TriSt-PU	Function

Table 5.1 FT2232H I/O States Channel A

5.1 FT2232H – Channel B Pins

FT2232H Channel B							
Pin Name	Pin Number	RESET# Low	Default	SUSPEND (Pull Down IO Pins in Suspend - Not Set)	SUSPEND (Pull Down IO Pins in USB Suspend - Set)	During Enumeration (out of reset prior to EEPROM read)	Active (device enumerated after eeprom read)
38	BDBUS0	TriSt	TXD	Function	TriSt-PD	TXD	Function
39	BDBUS1	TriSt-PU	RXD	Function	TriSt-PD	RXD	Function
40	BDBUS2	TriSt	RTS#	Function	TriSt-PD	RTS#	Function
41	BDBUS3	TriSt-PU	CTS#	Function	TriSt-PD	CTS#	Function
43	BDBUS4	TriSt	DTR#	Function	TriSt-PD	DTR#	Function
44	BDBUS5	TriSt-PU	DSR#	Function	TriSt-PD	DSR#	Function
45	BDBUS6	TriSt-PU	DCD#	Function	TriSt-PD	DCD#	Function
46	BDBUS7	TriSt-PU	RI#	Function	TriSt-PD	RI#	Function
48	BCBUS0	TriSt	TXDEN	Function	TriSt-PD	TXDEN	Function
52	BCBUS1	TriSt-PU	TriSt-PU	Function	TriSt-PD	TriSt-PU	Function
53	BCBUS2	TriSt-PU	TriSt-PU	Function	TriSt-PD	TriSt-PU	Function
54	BCBUS3	TriSt-PU	TriSt-PU	Function	TriSt-PD	TriSt-PU	Function
55	BCBUS4	TriSt-PU	TriSt-PU	Function	TriSt-PD	TriSt-PU	Function
57	BCBUS5	TriSt-PU	TriSt-PU	Function	TriSt-PD	TriSt-PU	Function
58	BCBUS6	TriSt-PU	TriSt-PU	Function	TriSt-PD	TriSt-PU	Function
59	BCBUS7	TriSt-PD	TriSt-PU	Function	TriSt-PD	TriSt-PU	Function

Table 5.2 FT2232H I/O States Channel B

5.2 FT2232H - Selected Function

FT2232H										
Pin		Pin functions (depends on configuration)								
Pin #	Pin Name	ASYNC Serial (RS232)	245 FIFO SYNC	245 FIFO	ASYNC Bit-bang	SYNC Bit-bang	MPSSE	Fast Serial interface	CPU Style FIFO	Host Bus Emulation
Channel A										
16	ADBUS0	TXD	D0	D0	D0	D0	TCK/SK	USES CHANNEL B	D0	AD0
17	ADBUS1	RXD	D1	D1	D1	D1	TDI/DO		D1	AD1
18	ADBUS2	RTS#	D2	D2	D2	D2	TDO/DI		D2	AD2
19	ADBUS3	CTS#	D3	D3	D3	D3	TMS/CS		D3	AD3
21	ADBUS4	DTR#	D4	D4	D4	D4	GPIOL0		D4	AD4
22	ADBUS5	DSR#	D5	D5	D5	D5	GPIOL1		D5	AD5
23	ADBUS6	DCD#	D6	D6	D6	D6	GPIOL2		D6	AD6
24	ADBUS7	RI#	D7	D7	D7	D7	GPIOL3		D7	AD7
26	ACBUS0	TXDEN	RXF#	RXF#	**	**	GPIOH0		CS#	A8
27	ACBUS1	**	TXE#	TXE#	WRSTB #	WRSTB #	GPIOH1		A0	A9
28	ACBUS2	**	RD#	RD#	RDSTB#	RDSTB#	GPIOH2		RD#	A10
29	ACBUS3	RXLED#	WR#	WR#	**	**	GPIOH3		WR#	A11
30	ACBUS4	TXLED#	SIWUA	SIWUA	SIWUA	SIWUA	GPIOH4		SIWUA	A12
32	ACBUS5	**	CLKOUT	**	**	**	GPIOH5		**	A13
33	ACBUS6	**	OE#	**	**	**	GPIOH6		**	A14
34	ACBUS7	**	**	**	**	**	GPIOH7		**	A15
Channel B										
38	BDBUS0	TXD		D0	D0	D0	TCK/SK	FSDI	D0	CS#
39	BDBUS1	RXD		D1	D1	D1	TDI/DO	FSCLK	D1	ALE
40	BDBUS2	RTS#		D2	D2	D2	TDO/DI	FSDO	D2	RD#
41	BDBUS3	CTS#		D3	D3	D3	TMS/CS	FSCTS	D3	WR#
43	BDBUS4	DTR#		D4	D4	D4	GPIOL0		D4	IORDY
44	BDBUS5	DSR#		D5	D5	D5	GPIOL1		D5	CLKOUT
45	BDBUS6	DCD#		D6	D6	D6	GPIOL2		D6	I/O0
46	BDBUS7	RI#		D7	D7	D7	GPIOL3		D7	I/O1
48	BCBUS0	TXDEN		RXF#	**	**	GPIOH0		CS#	**
52	BCBUS1	**		TXE#	WRSTB #	WRSTB #	GPIOH1		A0	**
53	BCBUS2	**		RD#	RDSTB#	RDSTB#	GPIOH2		RD#	**
54	BCBUS3	RXLED#		WR#	**	**	GPIOH3		WR#	**
55	BCBUS4	TXLED#		SIWUB	SIWUB	SIWUB	GPIOH4	SIWUB	SIWUB	**
57	BCBUS5	**		**	**	**	GPIOH5		**	**
58	BCBUS6	**		**	**	**	GPIOH6		**	**
59	BCBUS7	PWRSVAV #	PWRSVAV #	PWRSVAV #	PWRSVAV #	PWRSVAV #	GPIOH7	PWRSVAV #	PWRSVAV #	PWRSVAV #

Table 5.3 FT2232H Selected functions

Pins marked ** default to tri-stated inputs with an internal 75KΩ (approx) pull up resistor to VCCIO.

6 FT4232H – Channel A Pins

FT2232H Channel A							
Pin Name	Pin Number	RESET# Low	Default	SUSPEND (Pull Down IO Pins in Suspend - Not Set)	SUSPEND (Pull Down IO Pins in USB Suspend - Set)	During Enumeration (out of reset prior to EEPROM read)	Active (device enumerated after eeprom read)
16	ADBUS0	TriSt-PU	TXD	TXD	TriSt-PD	TXD	TXD
17	ADBUS1	TriSt-PU	RXD	RXD	TriSt-PD	RXD	RXD
18	ADBUS2	TriSt-PU	RTS#	RTS#	TriSt-PD	RTS#	RTS#
19	ADBUS3	TriSt-PU	CTS#	CTS#	TriSt-PD	CTS#	CTS#
21	ADBUS4	TriSt-PU	DTR#	DTR#	TriSt-PD	DTR#	DTR#
22	ADBUS5	TriSt-PU	DSR#	DSR#	TriSt-PD	DSR#	DSR#
23	ADBUS6	TriSt-PU	DCD#	DCD#	TriSt-PD	DCD#	DCD#
24	ADBUS7	TriSt-PU	RI#	Selection	TriSt-PD	RI#	Selection

Table 6.1 FT4232H I/O States Channel A

6.1 FT4232H – Channel B Pins

FT4232H Channel B							
Pin Name	Pin Number	RESET# Low	Default	SUSPEND (Pull Down IO Pins in Suspend - Not Set)	SUSPEND (Pull Down IO Pins in USB Suspend - Set)	During Enumeration (out of reset prior to EEPROM read)	Active (device enumerated after eeprom read)
26	BDBUS0	TriSt-PU	TXD	TXD	TriSt-PD	TXD	TXD
27	BDBUS1	TriSt-PU	RXD	RXD	TriSt-PD	RXD	RXD
28	BDBUS2	TriSt-PU	RTS#	RTS#	TriSt-PD	RTS#	RTS#
29	BDBUS3	TriSt-PU	CTS#	CTS#	TriSt-PD	CTS#	CTS#
30	BDBUS4	TriSt-PU	DTR#	DTR#	TriSt-PD	DTR#	DTR#
32	BDBUS5	TriSt-PU	DSR#	DSR#	TriSt-PD	DSR#	DSR#
33	BDBUS6	TriSt-PU	DCD#	DCD#	TriSt-PD	DCD#	DCD#
34	BDBUS7	TriSt-PU	RI#	Selection	TriSt-PD	RI#	Selection

Table 6.2 FT4232H I/O States Channel B

6.2 FT4232H – Channel C Pins

FT4232H Channel C							
Pin Name	Pin Number	RESET# Low	Default	SUSPEND (Pull Down IO Pins in Suspend - Not Set)	SUSPEND (Pull Down IO Pins in USB Suspend - Set)	During Enumeration (out of reset prior to EEPROM read)	Active (device enumerated after eeprom read)
48	CDBUS0	TriSt-PU	TXD	TXD	TriSt-PD	TXD	TXD
52	CDBUS1	TriSt-PU	RXD	RXD	TriSt-PD	RXD	RXD
53	CDBUS2	TriSt-PU	RTS#	RTS#	TriSt-PD	RTS#	RTS#
54	CDBUS3	TriSt-PU	CTS#	CTS#	TriSt-PD	CTS#	CTS#
55	CDBUS4	TriSt-PU	DTR#	DTR#	TriSt-PD	DTR#	DTR#
57	CDBUS5	TriSt-PU	DSR#	DSR#	TriSt-PD	DSR#	DSR#
58	CDBUS6	TriSt-PU	DCD#	DCD#	TriSt-PD	DCD#	DCD#
59	CDBUS7	TriSt-PU	RI#	Selection	TriSt-PD	RI#	Selection

Table 6.3 FT4232H I/O States Channel C

6.3 FT4232H – Channel D Pins

FT4232H Channel D							
Pin Name	Pin Number	RESET# Low	Default	SUSPEND (Pull Down IO Pins in Suspend - Not Set)	SUSPEND (Pull Down IO Pins in USB Suspend - Set)	During Enumeration (out of reset prior to EEPROM read)	Active (device enumerated after eeprom read)
26	DDBUS0	TriSt-PU	TXD	TXD	TriSt-PD	TXD	TXD
27	DDBUS1	TriSt-PU	RXD	RXD	TriSt-PD	RXD	RXD
28	DDBUS2	TriSt-PU	RTS#	RTS#	TriSt-PD	RTS#	RTS#
29	DDBUS3	TriSt-PU	CTS#	CTS#	TriSt-PD	CTS#	CTS#
30	DDBUS4	TriSt-PU	DTR#	DTR#	TriSt-PD	DTR#	DTR#
32	DDBUS5	TriSt-PU	DSR#	DSR#	TriSt-PD	DSR#	DSR#
33	DDBUS6	TriSt-PU	DCD#	DCD#	TriSt-PD	DCD#	DCD#
34	DDBUS7	TriSt-PD	RI#	Selection	TriSt-PD	RI#	Selection

Table 6.4 FT4232H I/O States Channel D

6.4 FT4232H - Selected Function

FT4232H					
Pins		Pin functions (depend on configuration)			
Pin #	Pin Name	ASYNC Serial (RS232)	ASYNC Bit-bang	SYNC Bit-bang	MPSSE
Channel A					
16	ADBUS0	TXD	D0	D0	TCK/SK
17	ADBUS1	RXD	D1	D1	TDI/DO
18	ADBUS2	RTS#	D2	D2	TDO/DI
19	ADBUS3	CTS#	D3	D3	TMS/CS
21	ADBUS4	DTR#	D4	D4	GPIOL0
22	ADBUS5	DSR#	D5	D5	GPIOL1
23	ADBUS6	DCD#	D6	D6	GPIOL2
24	ADBUS7	RI#/ TXDEN*	D7	D7	GPIOL3
Channel B					
26	BDBUS0	TXD	D0	D0	TCK/SK
27	BDBUS1	RXD	D1	D1	TDI/DO
28	BDBUS2	RTS#	D2	D2	TDO/DI
29	BDBUS3	CTS#	D3	D3	TMS/CS
30	BDBUS4	DTR#	D4	D4	GPIOL0
32	BDBUS5	DSR#	D5	D5	GPIOL1
33	BDBUS6	DCD#	D6	D6	GPIOL2
34	BDBUS7	RI#/ TXDEN*	D7	D7	GPIOL3
Channel C					
38	CDBUS0	TXD	D0	D0	RS232 or Bit-Bang interface
39	CDBUS1	RXD	D1	D1	RS232 or Bit-Bang interface
40	CDBUS2	RTS#	D2	D2	RS232 or Bit-Bang interface
41	CDBUS3	CTS#	D3	D3	RS232 or Bit-Bang interface
43	CDBUS4	DTR#	D4	D4	RS232 or Bit-Bang interface
44	CDBUS5	DSR#	D5	D5	RS232 or Bit-Bang interface
45	CDBUS6	DCD#	D6	D6	RS232 or Bit-Bang interface
46	CDBUS7	RI#/ TXDEN*	D7	D7	RS232 or Bit-Bang interface
Channel D					
48	DDBUS0	TXD	D0	D0	RS232 or Bit-Bang interface
52	DDBUS1	RXD	D1	D1	RS232 or Bit-Bang interface
53	DDBUS2	RTS#	D2	D2	RS232 or Bit-Bang interface
54	DDBUS3	CTS#	D3	D3	RS232 or Bit-Bang interface
55	DDBUS4	DTR#	D4	D4	RS232 or Bit-Bang interface
57	DDBUS5	DSR#	D5	D5	RS232 or Bit-Bang interface
58	DDBUS6	DCD#	D6	D6	RS232 or Bit-Bang interface
59	DDBUS7	RI#/ TXDEN*	D7	D7	RS232 or Bit-Bang interface

Table 6.5 Selected Function

7 FT2232D – Channel A Pins

FT2232D Channel A							
Pin Name	Pin Number	RESET# Low	Default	SUSPEND (Pull Down IO Pins in Suspend - Not Set)	SUSPEND (Pull Down IO Pins in USB Suspend - Set)	During Enumeration (out of reset prior to EEPROM read)	Active (device enumerated after eeprom read)
24	ADBUS0	TriSt	TXD	Function	TriSt- PD	TriSt	Function
23	ADBUS1	TriSt-PU	RXD	Function	TriSt- PD	TriSt-PU	Function
22	ADBUS2	TriSt	RTS#	Function	TriSt- PD	TriSt	Function
21	ADBUS3	TriSt-PU	CTS#	Function	TriSt- PD	TriSt-PU	Function
20	ADBUS4	TriSt	DTR#	Function	TriSt- PD	TriSt	Function
19	ADBUS5	TriSt-PU	DSR#	Function	TriSt- PD	TriSt-PU	Function
17	ADBUS6	TriSt-PU	DCD#	Function	TriSt- PD	TriSt-PU	Function
16	ADBUS7	TriSt-PU	RI#	Function	TriSt- PD	TriSt-PU	Function
15	ACBUS0	TriSt	TXDEN	Function	TriSt- PD	TriSt	Function
13	ACBUS1	TriSt	SLEEP#	Function	TriSt- PD	TriSt	Function
12	ACBUS2	TriSt-PU	RXLED#	Function	TriSt- PD	TriSt-PU	Function
11	ACBUS3	TriSt-PU	TXLED#	Function	TriSt- PD	TriSt-PU	Function

Table 7.1 FT2232D I/O States Channel A

7.1 FT2232D – Channel B Pins

FT2232D Channel B							
Pin Name	Pin Number	RESET# Low	Default	SUSPEND (Pull Down IO Pins in Suspend - Not Set)	SUSPEND (Pull Down IO Pins in USB Suspend - Set)	During Enumeration (out of reset prior to EEPROM read)	Active (device enumerated after eeprom read)
40	BDBUS0	TriSt	TXD	Function	TriSt- PD	TriSt	Function
39	BDBUS1	TriSt-PU	RXD	Function	TriSt- PD	TriSt-PU	Function
38	BDBUS2	TriSt	RTS#	Function	TriSt- PD	TriSt	Function
37	BDBUS3	TriSt-PU	CTS#	Function	TriSt- PD	TriSt-PU	Function
36	BDBUS4	TriSt	DTR#	Function	TriSt- PD	TriSt	Function
35	BDBUS5	TriSt-PU	DSR#	Function	TriSt- PD	TriSt-PU	Function
33	BDBUS6	TriSt-PU	DCD#	Function	TriSt- PD	TriSt-PU	Function
32	BDBUS7	TriSt-PU	RI#	Function	TriSt- PD	TriSt-PU	Function
30	BCBUS0	TriSt	TXDEN	Function	TriSt- PD	TriSt	Function
29	BCBUS1	TriSt	SLEEP#	Function	TriSt- PD	TriSt	Function
28	BCBUS2	TriSt-PU	RXLED#	Function	TriSt- PD	TriSt-PU	Function
27	BCBUS3	TriSt-PU	TXLED#	Function	TriSt- PD	TriSt-PU	Function

Table 7.2 FT2232D I/O States Channel B

7.2 FT2232D - Selected Function – Channel A

Pin#	Generic Pin name	Pin Definitions by Chip Mode **Note 1						
		232 UART Mode	245 FIFO	Enhanced Asynchronous and Synchronous Serial	MPSSE **Note 3	MCU Host Bus Emulation Mode **Note 4	Fast Opto-Isolated Serial Mode	CPU FIFO Interface Mode
24	ADBUS0	TXD	D0	D0	TCK/SK AD0	**Note 2	D0	D0
23	ADBUS1	RXD	D1	D1	TDI/D0	AD1	D1	D1
22	ADBUS2	RTS#	D2	D2	TDO/DI	AD2	D2	D2
21	ADBUS3	CTS#	D3	D3	TMS/CS AD3	D3		D3
20	ADBUS4	DTR#	D4	D4	GPIOL0	AD4	D4	D4
19	ADBUS5	DSR#	D5	D5	GPIOL1	AD5	D5	D5
17	ADBUS6	DCD#	D6	D6	GPIOL2	AD6	D6	D6
16	ADBUS7	RI#	D7	D7	GPIOL3	AD7	D7	D7
15	ACBUS0	TXDEN	RXF#	WR# **Note 5	GPIOH0	I/O0	CS#	CS#
13	ACBUS1	SLEEP#	TXE#	RD# **Note 5	GPIOH1	I/O1	A0	A0
12	ACBUS2	RXLED#	RD#	WR# **Note 6	GPIOH2	IORDY	RD#	RD#
24	ADBUS0	TXD	D0	D0	TCK/SK AD0	**Note 2	D0	
11	ACBUS3	TXLED#	WR	RD# **Note 6	GPIOH3	OSC	WR#	WR#

Table 7.3 Pin Definition by Chip Mode - Channel A

****Note 1:** 232 UART, 245 FIFO, CPU FIFO Interface, and Fast Opto-Isolated modes are enabled in the external EEPROM. Enhanced Asynchronous and Synchronous Bit-Bang modes, MPSSE, and MCU Host Bus Emulation modes are enabled using the driver command set bit mode.

****Note 2:** Channel A can be configured in another IO mode if channel B is in Fast Opto-Isolated Serial Mode. If both Channel A and Channel B are in Fast Opto-Isolated Serial Mode all of the IO will be on Channel B.

****Note 3:** MPSSE is Channel A only.

****Note 4:** MCU Host Bus Emulation requires both Channels.

****Note 5:** The Bit-Bang Mode (synchronous and asynchronous) WR# and RD# strobes are on these pins when the main Channel mode is 245 FIFO, CPU FIFO interface, or Fast Opto-Isolated Serial Modes.

****Note 6:** The Bit-Bang Mode (synchronous and asynchronous) WR# and RD# strobes are on these pins when the main Channel mode is 232 UART Mode.

7.3 FT2232D - Selected Function – Channel B

Pin#	Generic Pin name	Pin Definitions by Chip Mode **Note 1						
		232 UART Mode	245 FIFO	Enhanced Asynchronous and Synchronous Serial	MPSSE **Note 3	MCU Host Bus Emulation Mode **Note 4	Fast Opto-Isolated Serial Mode	CPU FIFO Interface Mode
40	BDBUS0	TXD	D0	D0	A8	FSDI	D0	D0
39	BDBUS1	RXD	D1	D1	A9	FSCLK	D1	D1
38	BDBUS2	RTS#	D2	D2	A10	FSDO	D2	D2
37	BDBUS3	CTS#	D3	D3	A11	FSCTS	D3	D3
36	BDBUS4	DTR#	D4	D4	A12	**Note 2	D4	D4
35	BDBUS5	DSR#	D5	D5	A13	D5		D5
33	BDBUS6	DCD#	D6	D6	A14	D6		D6
32	BDBUS7	RI#	D7	D7	A15	D7		D7
30	BCBUS0	TXDEN	RXF#	WR# **Note 7	CS#	CS#		CS#
29	BCBUS1	SLEEP#	TXE#	RD# **Note 7	ALE	A0		A0
28	BCBUS2	RXLED#	RD#	WR# **Note 6	RD#	RD#		RD#
27	BCBUS3	TXLED#	WR	RD# **Note 6	WR#	WR#		WR#

Table 7.4 Pin Definition by Chip Mode - Channel B

****Note 1:** 232 UART, 245 FIFO, CPU FIFO Interface, and Fast Opto-Isolated modes are enabled in the external EEPROM. Enhanced Asynchronous and Synchronous Bit-Bang modes, MPSSE, and MCU Host Bus Emulation modes are enabled using the driver command set bit mode.

****Note 2:** Channel A can be configured in another IO mode if channel B is in Fast Opto-Isolated Serial Mode. If both Channel A and Channel B are in Fast Opto-Isolated Serial Mode all of the IO will be on Channel B.

****Note 3:** MPSSE is Channel A only.

****Note 4:** MCU Host Bus Emulation requires both Channels.

****Note 5:** The Bit-Bang Mode (synchronous and asynchronous) WR# and RD# strobes are on these pins when the main Channel mode is 245 FIFO, CPU FIFO interface, or Fast Opto-Isolated Serial Modes.

****Note 6:** The Bit-Bang Mode (synchronous and asynchronous) WR# and RD# strobes are on these pins when the main Channel mode is 232 UART Mode.

****Note 7:** The Bit-Bang Mode (synchronous and asynchronous) WR# and RD# strobes are on these pins when the main Channel mode is 245 FIFO, CPU FIFO interface. Bit-Bang mode is not available on Channel B when Fast Opto-Isolated Serial Mode is enabled.

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Appendix A – References

Document References

[FT232R USB UART IC Data Sheet](#)

[FT245R USB FIFO Data Sheet](#)

[FT232H Single Channel Hi-Speed USB to Multipurpose UART/FIFO IC](#)

[FT2232H Hi-Speed Dual USB UART/FIFO IC Data Sheet](#)

[FT4232H Hi-Speed Quad USB UART IC Data Sheet](#)

[FT2232D Dual USB UART/FIFO IC Data Sheet](#)

Acronyms and Abbreviations

Terms	Description
USB	Universal Serial Bus
USB-IF	USB Implementers Forum

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Appendix C – Revision History

Document Title: AN_184 FTDI Device Input Output pin States
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Product Page: <http://www.ftdichip.com/FTProducts.htm>
Document Feedback: [Send Feedback](#)

Revision	Changes	Date
1.0	Initial Release	2011-11-24