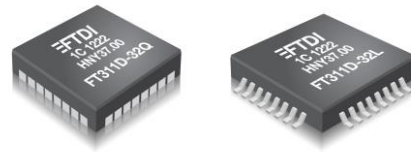


Future Technology Devices International Ltd.

FT311D (USB Android Host IC)



The FT311D is a Full Speed USB host specifically targeted at providing access to peripheral hardware from an Android platform with a USB device port. The device will bridge the USB port to six user selectable interface types and has the following advanced features:

- Single chip USB to selectable interface.
- Entire USB protocol handled on the chip. No USB specific firmware programming required.
- Interface options selectable via 3 mode select pins.
- 7 GPIO lines interface option
- Basic UART interface with RXD, TXD, RTS, CTS pins option.
- TX_ACTIVE signal for controlling transceivers on RS485 interfaces.
- 4 PWM channels option.
- I²C master interface option.
- SPI Slave interface option supporting modes 0, 1, 2 and 3 with MSB/LSB options
- SPI Master interface option supporting modes 0, 1, 2 and 3 with MSB/LSB options.
- USB error indicator pin
- Suitable for use on any Android platform supporting Android Open Accessory Mode (Typically 3.1 onwards, however some platforms may port Open Accessory Mode to version 2.3.4)
- 12MHz oscillator using external crystal.
- Integrated power-on-reset circuit.
- +3V3 Single Supply Operation with 5V tolerant inputs.
- USB 2.0 Full Speed compatible.
- Extended operating temperature range; -40°C to 85°C.
- Available in compact Pb-free 32 Pin LQFP and QFN packages (both RoHS compliant).

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1 Typical Applications

- Connecting Android phones to USB accessories
- Connecting Android tablets to USB accessories
- Controlling instrumentation from Android devices.
- Home automation via Android devices
- Data logging from USB accessories
- Connecting serial printing devices to Android devices

1.1 Part Numbers

| Part Number | Package |
|----------------|-------------|
| FT311D-32Q1C-x | 32 Pin QFN |
| FT311D-32L1C-x | 32 Pin LQFP |

Note: Packing codes for x is:

- R: Taped and Reel, QFN 3,000pcs per reel, LQFP 1500 pcs per reel.
- (no suffix): Tray packing, 260pcs per tray QFN, 250 pcs per tray LQFP

For example: FT311D-32Q1C-R is 3,000pcs QFN taped and reel packing

1.2 USB Compliant

At the time of writing this datasheet, the FT311D was still to complete USB compliancy testing.

2 FT311D Block Diagram

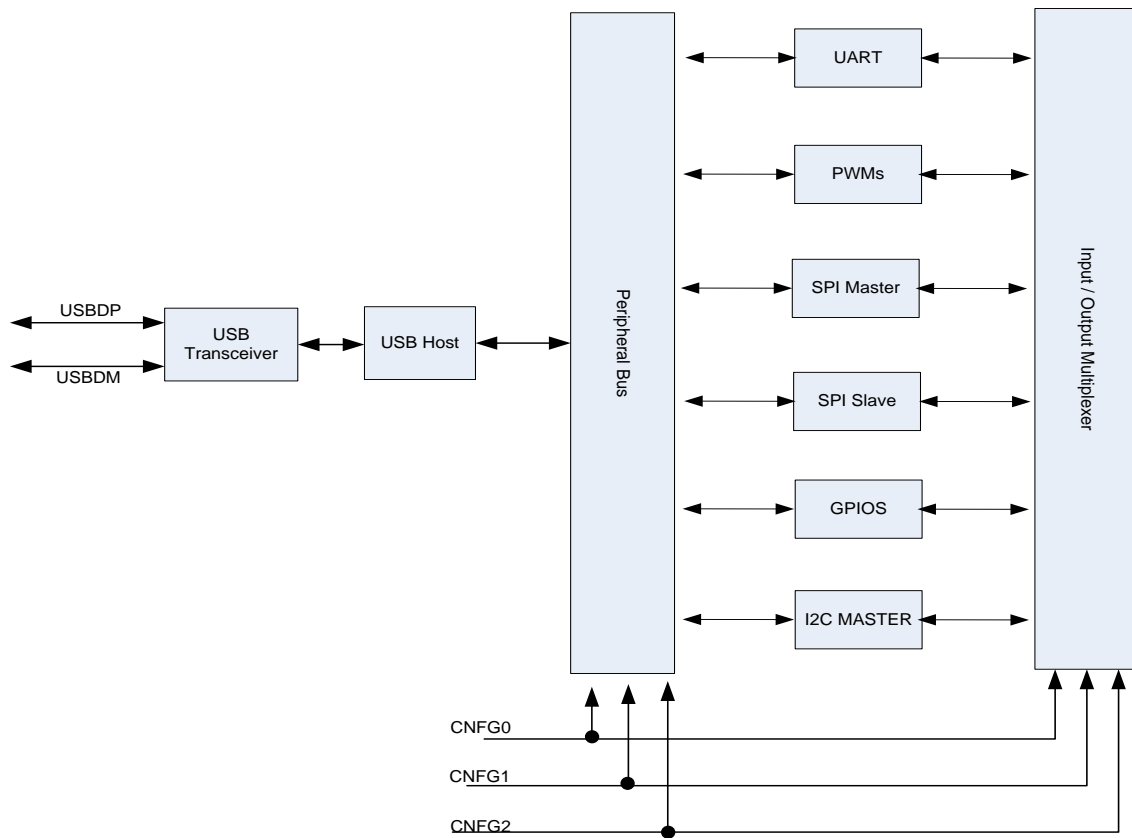


Figure 2.1 FT311D Block Diagram

For a description of each function please refer to Section 4.

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3 Device Pin Out and Signal Description

3.1 Package Symbol

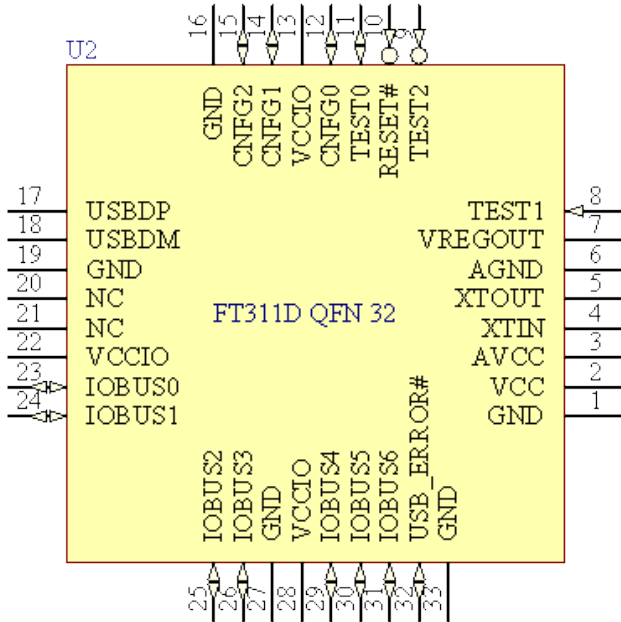


Figure 3.1 QFN Schematic Symbol

Note the pinout is the same for the QFN and LQFP packages.

3.1.1 Package PinOut Description

Note: # denotes an active low signal.

| Pin No. | Name | Type | Description |
|--------------|-----------------|--------------|--|
| 2 | 3.3V VREGIN | POWER Input | 3V3 supply to IC internal 1V8 regulator |
| 3 | 1.8V VCC PLL IN | POWER Input | 1V8 supply to IC core |
| 13, 22, 28 | VCCIO | POWER Input | 3V3 supply for the IO cells |
| 7 | VREGOUT | POWER Output | 1V8 output. May be used as input source for pin 3. |
| 1,6,16,19,27 | GND | POWER Input | 0V Ground input. |

Table 3.1 Power and Ground

| Pin No. | Name | Type | Description |
|---------|------------|--------------|---|
| 17 | USBDP | INPUT/OUTPUT | USB Data Signal Plus. |
| 18 | USBDM | INPUT/OUTPUT | USB Data Signal Minus. |
| 4 | XTIN | INPUT | Input to 12MHz Oscillator Cell. Connect 12MHz crystal across pins 4 and 5. |
| 5 | XTOUT | OUTPUT | Output from 12MHz Oscillator Cell. Connect 12MHz crystal across pins 4 and 5. |
| 8 | TEST1 | INPUT | For internal use. Pull to GND |
| 9 | TEST2 | INPUT | For factory use. Pull to 3V3. |
| 10 | RESET# | INPUT | Reset input (active low). |
| 20, 21 | NC | - | No connect pins. Leave unterminated. |
| 11 | TEST0 | OUTPUT | Active low signal that may be used to control a switch for enabling power to the USB port pin 1 (VBUS). |
| 12 | CNFG0 | INPUT | Configuration pin 0 used to select between GPIO,UART,PWM,I ² C and SPI. Pull to Ground = Logic '0'(No external resistor needed) Leave Open = Logic '1' (Internal Pull up is present) |
| 14 | CNFG1 | INPUT | Configuration pin 1 used to select between GPIO,UART,PWM,I ² C and SPI. Pull to Ground = Logic '0'(No external resistor needed) Leave Open = Logic '1' (Internal Pull up is present) |
| 15 | CNFG2 | INPUT | Configuration pin 2 used to select between GPIO,UART,PWM,I ² C and SPI. Pull to Ground = Logic '0'(No external resistor needed) Leave Open = Logic '1' (Internal Pull up is present) |
| 32 | USB_ERROR# | OUTPUT | Output signal to indicate a problem with the USB connection |

Table 3.2 Common Function pins

| Pin No. | Name | Type | Description |
|---------|--------|--------------|---|
| 23 | IOBUS0 | INPUT/OUTPUT | I/O signal. Function depends on CNFG pin setting. See table 3.4 |
| 24 | IOBUS1 | INPUT/OUTPUT | I/O signal. Function depends on CNFG pin setting. See table 3.4 |
| 25 | IOBUS2 | INPUT/OUTPUT | I/O signal. Function depends on CNFG pin setting. See table 3.4 |
| 26 | IOBUS3 | INPUT/OUTPUT | I/O signal. Function depends on CNFG pin setting. See table 3.4 |
| 29 | IOBUS4 | INPUT/OUTPUT | I/O signal. Function depends on CNFG pin setting. See table 3.4 |
| 30 | IOBUS5 | INPUT/OUTPUT | I/O signal. Function depends on CNFG pin setting. See table 3.4 |

| Pin No. | Name | Type | Description |
|---------|--------|--------------|---|
| 31 | IOBUS6 | INPUT/OUTPUT | I/O signal. Function depends on CNFG pin setting. See table 3.4 |

Table 3.3 Interface Pins

Notes:

1. When used in Input Mode, the input pins are pulled to VCCIO via internal 75kΩ (approx.) resistors.

3.2 Interface Selection

The FT311D has multiple interfaces available for connecting to external devices. The resources available are GPIO, UART, PWM, I2C(Master), SPI(Slave) and SPI(Master). The selection of what interface the user requires is configured using the CNFG0, CNFG1 and CNFG2 input pins as per table 3.4.

| CNFG2 | CNFG1 | CNFG0 | Mode |
|------------|------------|------------|--------------|
| GND | GND | GND | GPIO |
| GND | GND | Leave Open | UART |
| GND | Leave Open | GND | PWM |
| GND | Leave Open | Leave Open | I2C (Master) |
| Leave Open | GND | GND | SPI (Slave) |
| Leave Open | GND | Leave Open | SPI (Master) |

Table 3.4 CBUS Configuration Control

Note 1: When left open the pin is a logic 1.

Note 2: Mode "110" is a factory test mode and should not be used.

Note 3: Mode "111" will default to GPIO mode.

3.2.1 Interface pinout

The actual pinout for each interface type is detailed in table 3.5

| Pin No | Pin Name | GPIO | UART | PWM | I2C (Master) | SPI (Slave) | SPI (Master) |
|--------|----------|-------|------------|------|--------------|-------------|--------------|
| 23 | IOBUS0 | GPIO0 | UART_TXD | PWM0 | I2C_CLK | - | - |
| 24 | IOBUS1 | GPIO1 | UART_RXD | PWM1 | I2C_DATA | - | - |
| 25 | IOBUS2 | GPIO2 | UART_RTS # | PWM2 | - | - | - |
| 26 | IOBUS3 | GPIO3 | UART_CTS # | PWM3 | - | SPI_S_SS0 | SPI_M_SS0 |

| Pin No | Pin Name | GPIO | UART | PWM | I2C (Master) | SPI (Slave) | SPI (Master) |
|--------|----------|-------|----------------|-----|--------------|-------------|--------------|
| 29 | IOBUS4 | GPIO4 | UART_TX_ACTIVE | - | - | SPI_S_CLK | SPI_M_CLK |
| 30 | IOBUS5 | GPIO5 | - | - | - | SPI_S_MOSI | SPI_M_MOSI |
| 31 | IOBUS6 | GPIO6 | - | - | - | SPI_S_MISO | SPI_M_MISO |

Table 3.5 I/O Configuration

4 Function Description

FT311D is FTDI's Android Accessory Mode integrated circuit device or Android Host. The FT311D behaves like a bridge between an Android device and the various I/O available. Selection of various modes is performed using CNFGx pins.

4.1 Key Features

Easy to use Android accessory IC translating the Device port of the android tablet into either GPIO, UART, PWM, I²C Master, SPI Slave or SPI Master capabilities

4.2 Functional Block Descriptions

The following paragraphs describe each function within FT311D. Please refer to the block diagram shown in **Figure 2.1**.

4.2.1 Peripheral Interface Modules

FT311D has six peripheral interface modules available for selection. Full descriptions of each module are provided in [Section 5](#).

- GPIO - General purpose I/O pins
- UART
- PWM
- I2C Master
- SPI Slave
- SPI Master

4.2.2 USB Transceivers

USB transceiver cells provide the physical USB device interface supporting USB 1.1 and USB 2.0 standards. Low-speed and full-speed USB data rates are supported. The output driver provides +3.3V level slew rate control signalling, whilst a differential receiver and two single ended receivers provide USB DATA IN, SE0 and USB Reset condition detection. These cells also include integrated internal pull-down resistors as required for host mode.

4.2.3 USB Host

These blocks handle the parallel-to-serial and serial-to-parallel conversion of the USB physical layer. This includes bit stuffing, CRC generation.

4.3 I/O Peripherals Signal Names

| Peripheral | Signal Name | Outputs | Inputs | Description |
|------------------|----------------|---------|--------|--|
| GPIO | gpio | 7 | 7 | General purpose I/O |
| UART | uart_txd | 1 | 0 | Transmit asynchronous data output |
| | uart_rts# | 1 | 0 | Request to send control output |
| | uart_rxd | 0 | 1 | Receive asynchronous data input |
| | uart_cts# | 0 | 1 | Clear to send control input |
| | uart_tx_active | 0 | 1 | UART active signal (typically used with RS485) |
| PWM | pwm | 4 | 0 | Pulse width modulation |
| I ² C | I2c_scl | 0 | 1 | I2C bus serial clock line - slave |
| | I2c_sda | 1 | 1 | I2C bus serial data line - slave |
| SPI Slave | spi_s_clk | 0 | 1 | SPI clock input |

| Peripheral | Signal Name | Outputs | Inputs | Description |
|------------|-------------|---------|--------|--|
| | spi_s_ss# | 0 | 1 | SPI slave select input |
| | spi_s_mosi | 1 | 1 | SPI master out serial in |
| | spi_s_miso | 1 | 0 | SPI master in slave out |
| SPI Master | spi_m_clk | 1 | 0 | SPI clock input - master |
| | spi_m_mosi | 1 | 1 | Master out slave in - master |
| | spi_m_miso | 0 | 1 | Master in slave out - master |
| | spi_m_ss_0# | 1 | 0 | Active low slave select 0 from master to slave 0 |

Table 4.1 I/O Peripherals Signal Names

Note: # is used to indicate an active low signal.

4.4 Default Mode Strings

When the USB port is connected to the Android USB port, the Android platform will determine which application to load based on the strings read from the FT311D. These strings are configurable with a Windows utility: FT311Configuration.exe available for download from the FTDI website at: http://www.ftdichip.com/Support/SoftwareExamples/Android/FT311Configuration_V010100.zip

Default values for the strings are set in the device as per Table 4.2

| Descriptor String | Default Value |
|---|---|
| Manufacturer | FTDI |
| Model (depends on GPIO Mode selection): | |
| GPIO | FTDIGPIODemo |
| UART | FTDIUARTDemo |
| PWM | FTDIPWMDemo |
| I ² C | FTDII2CDemo |
| SPI Slave | FTDISPISlaveDemo |
| SPI Master | FTDISPIMasterDemo |
| Version | 1.0 |
| Serial | VinculumAccessory1 |
| Description URL | http://www.ftdichip.com |

Table 4.2 Default Descriptor Strings

5 Peripheral Interfaces

In addition to the USB Host, FT311D contains the following peripheral interfaces:

- General Purpose Input Output (GPIO)
- Universal Asynchronous Receiver Transmitter (UART)
- Four Pulse Width Modulation blocks (PWM)
- I²C Master
- Serial Peripheral Interface (SPI) Slave
- Serial Peripheral Interface (SPI) Master

Note: Only one interface may be selected at any time.

The modes are selected by setting the CNFGx pins.

The following sections describe each peripheral in detail.

5.1 General Purpose Input Output

FT311D provides up to 7 configurable Input/Output pins. All pins are independently configurable to be either inputs or outputs.

5.2 UART Interface

When the peripheral interface is configured in UART mode, the interface implements a standard asynchronous serial UART port with flow control, for example RS232/422/485. The UART can support baud rates from 300 baud to 6 Mbaud.

Data transfer uses NRZ (Non-Return to Zero) data format consisting of 1 start bit, 7 or 8 data bits, an optional parity bit, and one or two stop bits. When transmitting the data bits, the least significant bit is transmitted first. Transmit and receive waveforms are illustrated in **Figure 5-1** and **Figure 5-2**:

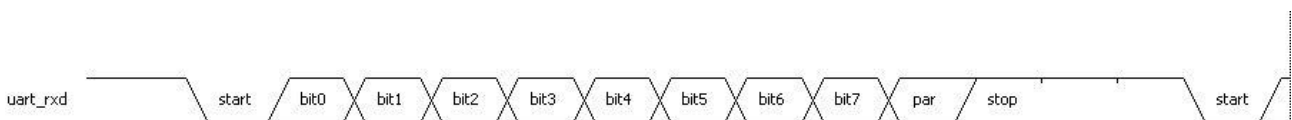


Figure 5-1 UART Receive Waveform

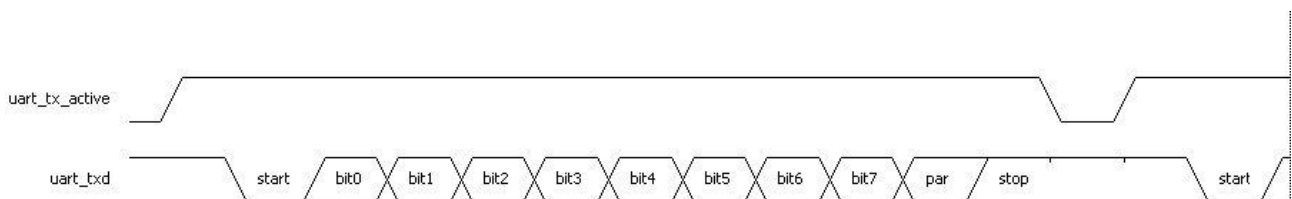


Figure 5-2 UART Transmit Waveform

Baud rate (default = 9600 baud), flow control settings (default = RTS/CTS), number of data bits (default=8), parity (default is no parity) and number of stop bits (default=1) are all configurable from the Android application. Please refer to [http://www.ftdichip.com/Support/Documents/ProgramGuides/FT31XD Android_programmer_guide\(FT_000532\).pdf](http://www.ftdichip.com/Support/Documents/ProgramGuides/FT31XD Android_programmer_guide(FT_000532).pdf) for further details.

uart_tx_active is transmit enable, this output may be used in RS485 designs to control the transmit of the line driver.

5.2.1 UART Mode Signal Descriptions

The UART signals are fixed on the I/O pins. Table 5.1 UART Interface, details the pins for each of the UART signals.

| Pin No | Name | Type | Description |
|--------|----------------|--------|--|
| 23 | uart_txd | Output | Transmit asynchronous data output |
| 24 | uart_rxd | Input | Receive asynchronous data input |
| 25 | uart_rts# | Output | Request to send control output |
| 26 | uart_cts# | Input | Clear to send control input |
| 29 | uart_tx_active | output | Transmit enable (typically used for RS485 designs) |

Table 5.1 UART Interface

Note:

The FT311D has to enumerate the Android device before receiving data from the UART device.

This can be implemented by disconnecting the UART TXD signal of external UART device connected to the FT311D uart_rxd signal until after the FT311D has established the USB link with Android device.

The connection sequence should be:

1. Connect FT311D to Android and complete enumeration.
2. Connect the TXD of UART device to FT311D's RXD then start to receive data.

There are two methods to implement this function:

1. When FT311D connects to the Android device and enumeration is completed, the USB_ERROR# will become Logic 0 (default Logic 1). This signal can be used to control the TTL gate (74LVC2G241, 74LVC1G125 or others) ON/OFF such that the TXD/RXD lines are connected/disconnected.

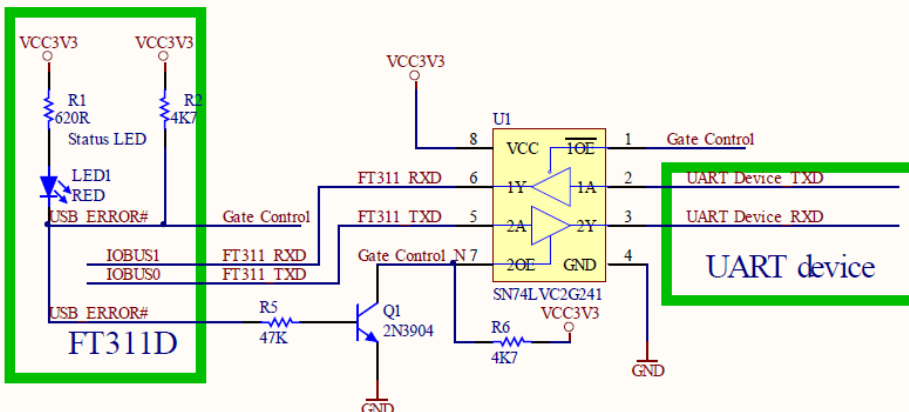


Figure 5-3 UART RXD and TXD connection gated by Enumeration

2. If the UART device has an enable pin(active high enable) such as on the GPS module, the USB_ERROR# can also be used. The USB_ERROR# pin may be inverted with an NPN BJT then connected to the enable pin of the GPS module.

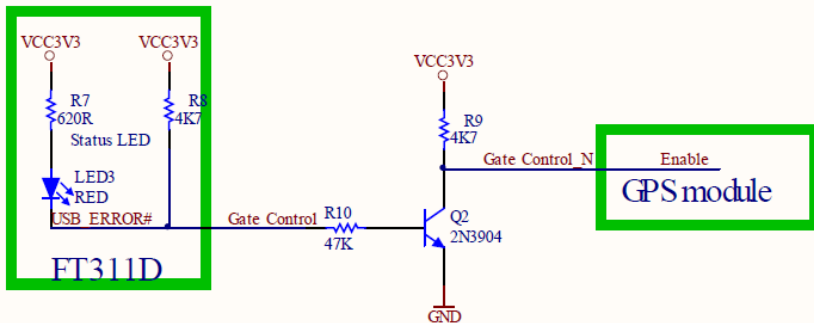


Figure 5-4 Inverting Gate Control signal to enable GPS module(active high enable)

5.3 Pulse Width Modulation

FT311D provides 4 Pulse Width Modulation (PWM) outputs. These can be used to generate PWM signals which can be used to control motors, DC/DC converters, AC/DC supplies, etc. Further information is available in an Application Note AN_140 - [Vinculum-II PWM Example](#).

The features of the PWM module are as follows:

- 4 PWM outputs
- Variable frequency
- Variable duty cycle

5.4 I2C

I²C (Inter Integrated Circuit) is a multi-master serial bus invented by Philips. I²C uses two bi-directional open-drain wires called serial data (SDA) and serial clock (SCL). Common I²C bus speeds are the 100 kbit/s standard mode (SM), 400 kbit/s fast mode (FM), 1 Mbit/s Fast mode plus (FM+), and 3.4 Mbit/s High Speed mode (HS)

An I²C bus node can operate either as a master or a slave:

- Master node – issues the clock and addresses slaves
- Slave node – receives the clock line and address.

FT311D provides an I2C master interface for connection to other I2C Slave interfaces up to 125kbit/s.

The master is initially in master transmit mode by sending a start bit followed by the 7-bit address of the slave it wishes to communicate with, which is finally followed by a single bit representing whether to write(0) to, or read(1) from the slave.

If the slave exists on the bus then it will respond with an ACK bit (active low for acknowledged) for that address. The master then continues in either transmit or receive mode (according to the read/write bit it sent), and the slave continues in its complementary mode (receive or transmit, respectively).

The address and the data bytes are sent most significant bit first. The start bit is indicated by a high-to-low transition of SDA with SCL high; the stop bit is indicated by a low-to-high transition of SDA with SCL high.

If the master has to write to the slave then it repeatedly sends a byte with the slave sending an ACK bit. (In this situation, the master is in master transmit mode and the slave is in slave receive mode.)

If the master has to read from the slave then it repeatedly receives a byte from the slave, the master sending an ACK bit after every byte but the last one. (In this situation, the master is in master receive mode and the slave is in slave transmit mode.)

The master then ends transmission with a stop bit, or it may send another START bit if it wishes to retain control of the bus for another transfer (a "combined message").

I²C defines three basic types of message, each of which begins with a START and ends with a STOP:

- Single message where a master writes data to a slave;
- Single message where a master reads data from a slave;
- Combined messages, where a master issues at least two reads and/or writes to one or more slaves

In a combined message, each read or write begins with a START and the slave address. After the first START, these are also called repeated START bits; repeated START bits are not preceded by STOP bits, which is how slaves know the next transfer is part of the same message.

Please refer to the I²C specification for more information on the protocol.

5.5 Serial Peripheral Interface – SPI Modes

The Serial Peripheral Interface Bus is an industry standard communications interface. Devices communicate in Master / Slave mode, with the Master initiating the data transfer.

FT311D has one master module and one slave module. Both the SPI master and slave module has four signals – clock, slave select, MOSI (master out – slave in) and MISO (master in – slave out). Table 5.2 lists how the signals are named in each module.

| Module | Signal Name | Type | Description |
|------------|-------------|--------|--|
| SPI Slave | spi_s_clk | Input | Clock input |
| | spi_s_ss# | Input | Active low slave select input |
| | spi_s_mosi | Input | Master out serial in |
| | spi_s_miso | Output | Master in slave out |
| SPI Master | spi_m_clk | Output | Clock output – master |
| | spi_m_mosi | Output | Master out slave in - master |
| | spi_m_miso | Input | Master in slave out - master |
| | spi_m_ss_0# | Output | Active low slave select 0 from master to slave 0 |

Table 5.2 SPI Signal Names

The SPI slave protocol by default does not support any form of handshaking. It is simply transferring 8 bit data.

5.5.1 SPI Clock Phase Modes

SPI interface has 4 unique modes of clock phase (CPHA) and clock polarity (CPOL), known as Mode 0, Mode 1, Mode 2 and Mode 3. Table 5.3 summarizes these modes and available interface and **Figure 5-5** is the function timing diagram.

For CPOL = 0, the base (inactive) level of SCLK is 0.

In this mode:

- When CPHA = 0, data is clocked in on the rising edge of SCLK, and data is clocked out on the falling edge of SCLK.
- When CPHA = 1, data is clocked in on the falling edge of SCLK, and data is clocked out on the rising edge of SCLK

For CPOL =1, the base (inactive) level of SCLK is 1.

In this mode:

- When CPHA = 0, data is clocked in on the falling edge of SCLK, and data is clocked out on the rising edge of SCLK
- When CPHA =1, data is clocked in on the rising edge of SCLK, and data is clocked out on the falling edge of SCLK.

| Mode | CPOL | CPHA |
|------|------|------|
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| 2 | 1 | 0 |
| 3 | 1 | 1 |

Table 5.3 - Clock Phase/Polarity Modes

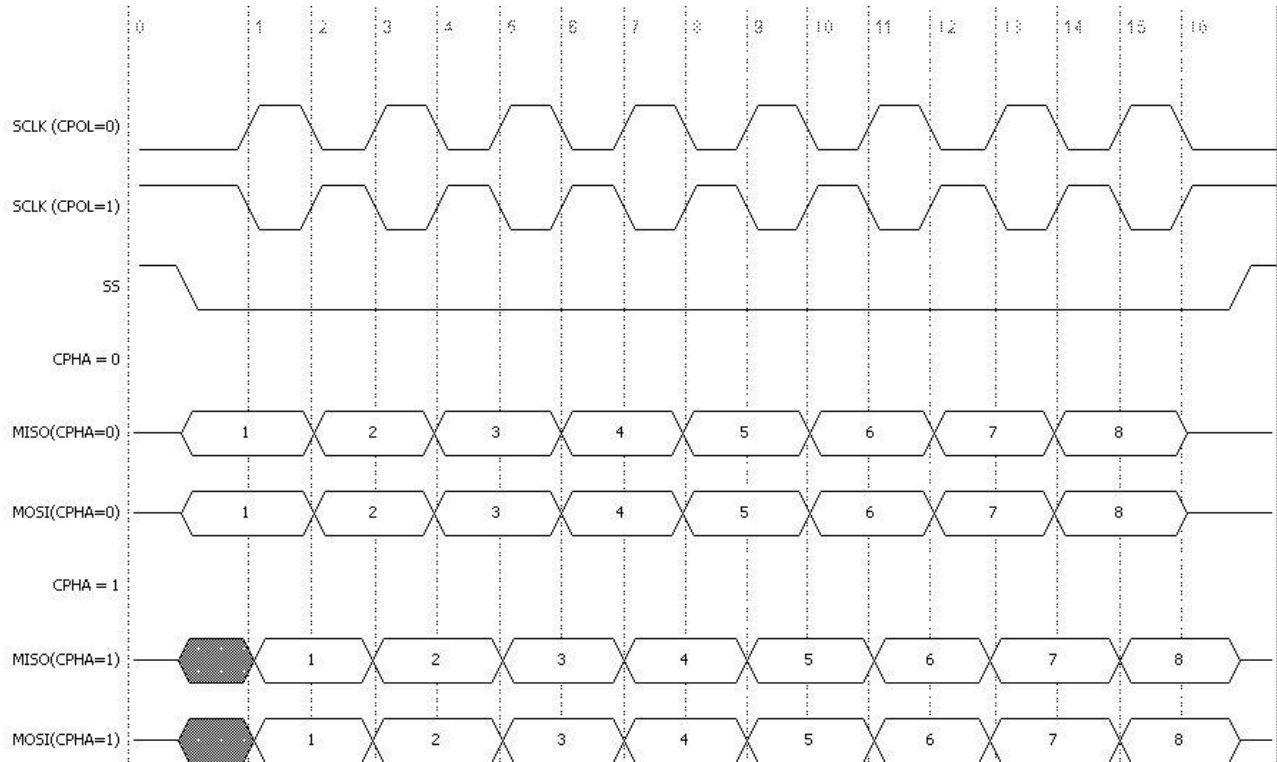


Figure 5-5 - SPI CPOL CPHA Function

5.5.2 Serial Peripheral Interface – Slave

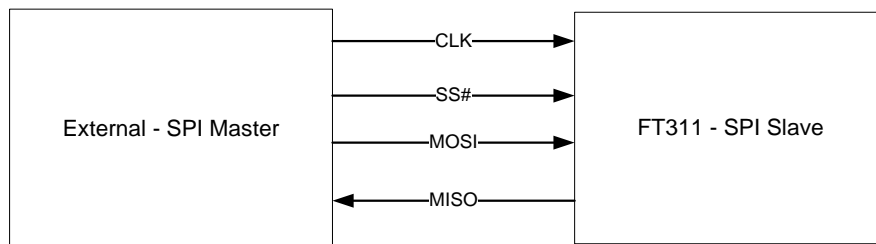


Figure 5-6 SPI Slave block diagram

FT311D has an SPI Slave module that uses four wire interfaces: MOSI, MISO, CLK and SS#. An SPI transfer can only be initiated by the SPI Master and begins with the slave select signal being asserted. This is followed by a data byte being clocked out with the master supplying CLK. The master always supplies the first byte, which is called a command byte. After this the desired number of data bytes are transferred before the transaction is terminated by the master de-asserting slave select. An SPI Master is able to abort a transfer at any time by de-asserting its SS# output. This will cause the Slave to end its current transfer and return to idle state.

5.5.2.1 SPI Slave Signal Descriptions

| Pin No | Name | Type | Description |
|--------|-------------|--------|--|
| 29 | spi_s0_clk | Input | Slave clock input |
| 30 | spi_s0_mosi | Input | Master Out Slave In Synchronous data from master to slave |
| 31 | spi_s0_miso | Output | Master In Slave Out Synchronous data from slave to master |
| 26 | spi_s0_ss# | Input | Slave select |

Table 5.4 Data and Control Bus Signal Mode Options - SPI Slave Interface

Note:

The FT311D has to enumerate the Android device before receiving data from the SPI master device. This can be implemented by disconnecting the SS# signal of SPI Host device until after the FT311D has established the USB link with Android device.

The connection sequence should be:

1. Connect FT311D to Android and complete enumeration.
2. Connect the SS# of SPI host to FT311D's SS# then start to communication.

There is a method to implement this function:

1. When FT311D connects to the Android device and enumeration is completed, the USB_ERROR# will become Logic 0 (default Logic 1). This signal can be used to control the TTL gate (74LVC2G241, 74LVC1G125 or others) ON/OFF such that the Both SS# lines are connected/disconnected.

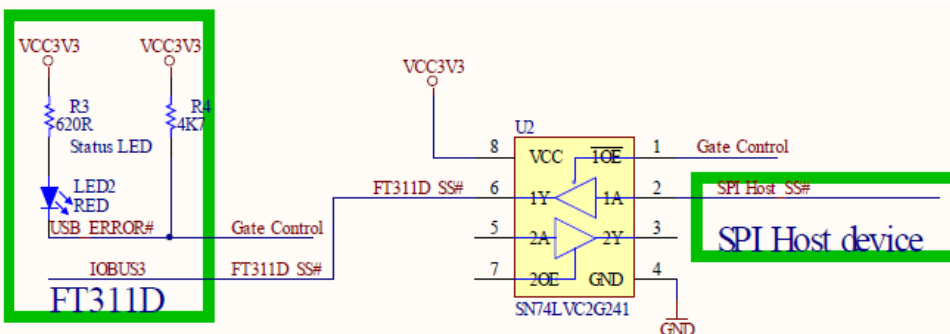


Figure 5-7 SPI Slave SS gated by Enumeration

5.5.3 Serial Peripheral Interface – SPI Master

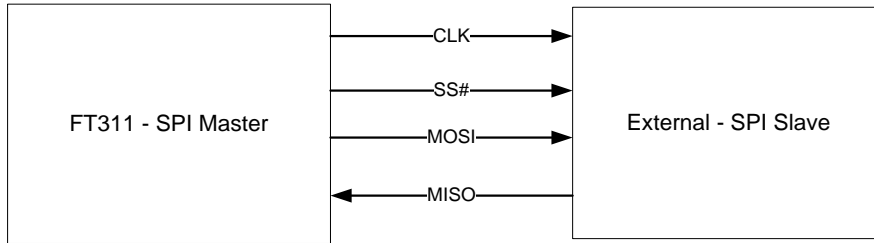


Figure 5-8 SPI Master block diagram

The SPI Master interface is used to interface to applications such as Real time clocks and audio codecs. The SPI Master provides the following features:

- Synchronous serial data link.
- Full and half duplex data transmission.
- Serial clock with programmable frequency, polarity and phase.
- One slave select output.

5.5.3.1 SPI Master Signal Descriptions.

Table 5.5 shows the SPI master signals and the pins

| Pin No | Name | Type | Description |
|--------|-------------|--------|--|
| 29 | spi_m_clk | Output | SPI master clock input |
| 30 | spi_m_mosi | Output | Master Out Slave In Synchronous data from master to slave |
| 31 | spi_m_miso | Input | Master In Slave Out Synchronous data from slave to master |
| 26 | spi_m_ss_0# | Output | Active low slave select 0 from master to slave |

Table 5.5 SPI Master Signal Names

The main purpose of the SPI Master block is to transfer data between an external SPI interface and the FT311D.

An SPI master interface transfer can only be initiated by the SPI Master and begins with the slave select signal being asserted. This is followed by a data byte being clocked out with the master supplying SCLK. The master typically supplies the first byte, which is called a command byte. After this the desired

number of data bytes are transferred before the transaction is terminated by the master de-asserting slave select. However the FT311D is simply a data pipe and no command is required by the FT311D itself. Any command protocol would be defined by the Android application.

The SPI Master will transmit on MOSI as well as receive on MISO during every data stage.

Figure 5-9 Typical SPI Master Timing and Table 5.6 SPI Master Timing show an example of this.

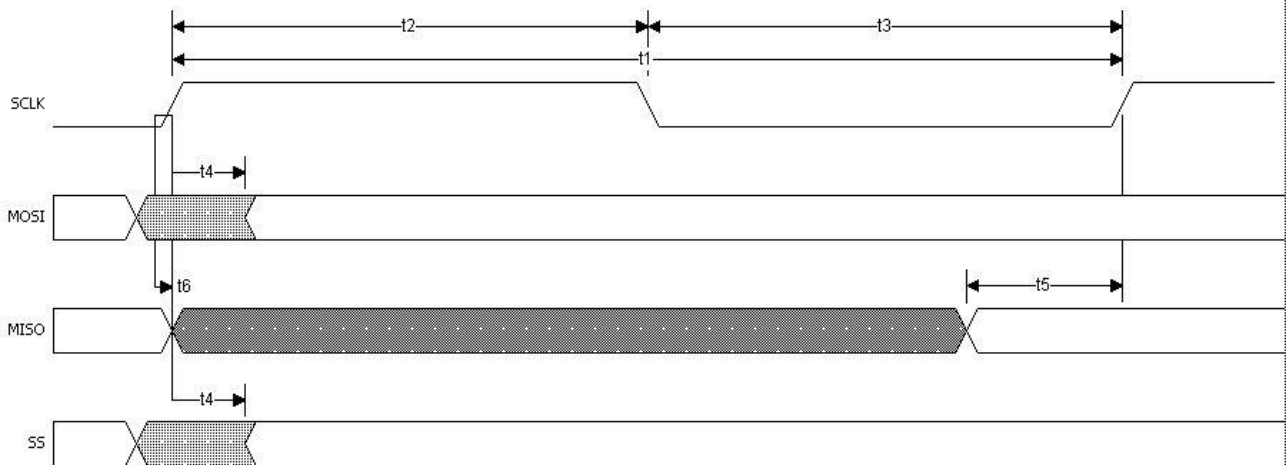


Figure 5-9 Typical SPI Master Timing

| Time | Description | Minimum | Typical | Maximum | Unit |
|------|--------------------------------------|---------|---------|---------|------|
| t1 | SCLK period | 39.68 | 41.67 | | ns |
| t2 | SCLK high period | 19.84 | 20.84 | 21.93 | ns |
| t3 | SCLK low period | 19.84 | 20.84 | 21.93 | ns |
| t4 | SCLK driving edge to MOSI/SS | -1.5 | | 3 | ns |
| t5 | MISO setup time to sample SCLK edge | | | 6.5 | ns |
| t6 | MISO hold time from sample SCLK edge | 0 | | | ns |

Table 5.6 SPI Master Timing

6 USB Error Detection

Pin 32 (IOBUS7) of the device is provided to indicate a problem has occurred with the USB connection. Typical errors include USB Device Not Supported, which would occur if the USB port was connected to a non-Android class device port e.g. the FT311D is not designed to host memory sticks or printers etc. USB Device Not Responding and Hub not supported would be reported also if connected to a hub. The signal states are as follows:

| Pin state | Definition |
|---------------------------|---|
| Logic 0 | Device connected to USB and functional |
| Logic 1 | Device not connected |
| One 50ms logic 0 pulse | Device not responding. This pulse occurs at plug-in and then the signal returns to logic 1. This then repeats at a 1 second interval. |
| Two 50ms logic 0 pulses | Device not supported. These pulses occur at plug-in and then the signal returns to logic 1. This then repeats at a 1 second interval. |
| Three 50ms logic 0 pulses | Hub not supported. These pulses occur at plug-in and then the signal returns to logic 1. This then repeats at a 1 second interval. |

Table 6.1 Error Detection

7 Absolute Maximum Ratings

The absolute maximum ratings for FT311D are shown in Table 7.1. These are in accordance with the Absolute Maximum Rating System (IEC 60134). Exceeding these may cause permanent damage to the device.

| Parameter | Value | Unit |
|---|---|---------------|
| Storage Temperature | -65°C to 150°C | Degrees C |
| Floor Life (Out of Bag) At Factory Ambient (30°C / 60% Relative Humidity) | 168 Hours (IPC/JEDEC J-STD-033A MSL Level 3 Compliant)* | Hours |
| Ambient Temperature (Power Applied) | -40°C to 85°C | Degrees C. |
| Vcc Supply Voltage | 0 to +3.63 | V |
| VCC_IO | 0 to +3.63 | V |
| VCC_PLL_IN | 0 to + 1.98 | V |
| DC Input Voltage - USBDP and USBDM | -0.5 to +(Vcc +0.5) | V |
| DC Input Voltage - High Impedance Bidirectional | -0.5 to +5.00 | V |
| DC Input Voltage - All other Inputs | -0.5 to +(Vcc +0.5) | V |
| DC Output Current - Outputs | 4 | mA |
| DC Output Current - Low Impedance Bidirectional | 4 | mA |

Table 7.1 Absolute Maximum Ratings

- * If devices are stored out of the packaging beyond this time limit the devices should be baked before use. The devices should be ramped up to a temperature of 125°C and baked for up to 17 hours.

7.1 DC Characteristics

DC Characteristics (Ambient Temperature -40°C to +125°C)

| Parameter | Description | Minimum | Typical | Maximum | Units | Conditions |
|-----------|-----------------------------------|---------|---------|---------|-------|------------------|
| Vcc1 | VCC Operating Supply Voltage | 2.97 | 3.3 | 3.63 | V | |
| Vcc2 | VCCIO Operating Supply Voltage | 2.97 | 3.3 | 3.63 | V | |
| VCC_PLL | VCC_PLL Operating Supply Voltage | 1.62 | 1.8 | 1.98 | V | |
| Icc1 | Operating Supply Current 48MHz | | 25 | | mA | Normal Operation |
| Icc2 | Operating Supply Current | | 128 | | μA | USB Suspend |

Table 7.2 Operating Voltage and Current

| Parameter | Description | Minimum | Typical | Maximum | Units | Conditions |
|-----------|---------------------------|---------|---------|---------|-------|----------------|
| Voh | Output Voltage High | 2.4 | | | V | I source = 8mA |
| Vol | Output Voltage Low | | | 0.4 | V | I sink = 8mA |
| Vin | Input Switching Threshold | | 1.5 | | V | |

Table 7.3 I/O Pin Characteristics

| Parameter | Description | Minimum | Typical | Maximum | Units | Conditions |
|-----------|------------------------------------|---------|---------|---------|-------|------------|
| UVoh | I/O Pins Static Output (High) | 2.8 | | | V | |
| UVol | I/O Pins Static Output (Low) | | | 0.3 | V | |
| UVse | Single Ended Rx Threshold | 0.8 | | 2.0 | V | |
| UCom | Differential Common Mode | 0.8 | | 2.5 | V | |

| | | | | | | |
|-------|--------------------------------|-----|---|---|------|--|
| UVdif | Differential Input Sensitivity | 0.2 | | | V | |
| UDrvZ | Driver Output Impedance | 3 | 6 | 9 | Ohms | |

Table 7.4 USB I/O Pin (USBDP, USBDM) Characteristics

| Parameter | Description | Minimum | Typical | Maximum | Units | Conditions |
|-----------------|---|---------|---------|---------|-------|---------------------------------|
| VCKK | Power supply of internal core cells and I/O to core interface | 1.62 | 1.8 | 1.98 | V | 1.8V power supply |
| VCC18IO | Power supply of 1.8V OSC pad | 1.62 | 1.8 | 1.98 | V | 1.8V power supply |
| T _J | Operating junction temperature | -40 | 25 | 125 | °C | |
| I _{in} | Input leakage current | -10 | ±1 | 10 | µA | I _{in} = VCC18IO or 0V |
| I _{oz} | Tri-state output leakage current | -10 | ±1 | 10 | µA | |

Table 7.5 Crystal Oscillator 1.8 Volts DC Characteristics

7.2 ESD and Latch-up Specifications

| Description | Specification |
|---------------------------|---------------|
| Human Body Mode (HBM) | ± 2000V |
| Machine mode (MM) | ± 200V |
| Charged Device Mode (CDM) | ± 500V |
| Latch-up | > ± 200mA |

Table 7.6 ESD and Latch-up Specifications

8 Application Examples

The following sections illustrate possible applications of the FT311D.

8.1 USB to GPIO Converter

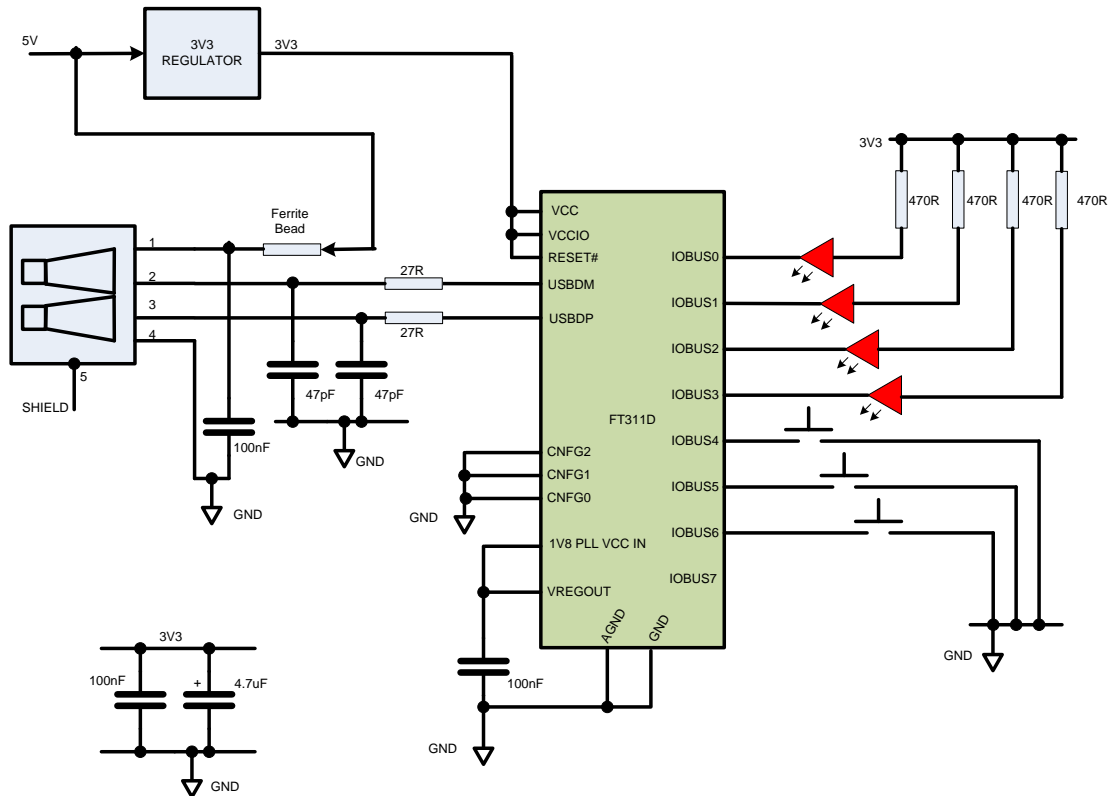


Figure 8.1 Application Example showing USB to GPIO Converter

This example shows the CNFGx pins set for mode 000 – GPIO.

IOBUS0-3 are configured as outputs by the Android application to control the LEDs.

IOBUS4-6 pins are configured as inputs to allow the buttons to control actions in the Android application.

8.2 USB to UART Converter

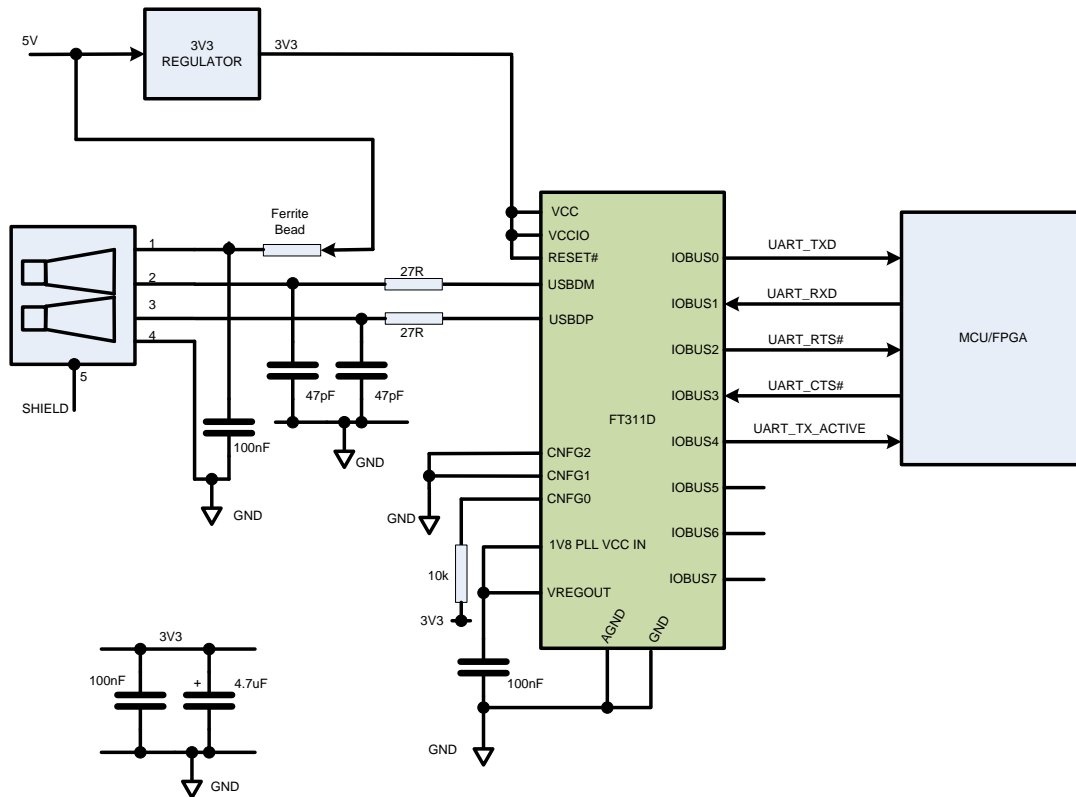


Figure 8.2 Application Example showing USB to UART Converter

This example shows the CNFGx pins set for mode 001 - UART.

The UART signals are at 3V3 level and may be used to drive directly into a FPGA or MCU with a 3V3 interface, or could be level shifted with an RS232, RS422 or RS485 transceiver. The UART_TX_ACTIVE signal is used mostly with RS485 transceivers to enable the transmit drivers.

The unused pins may be left unterminated.

8.3 USB to PWM Converter

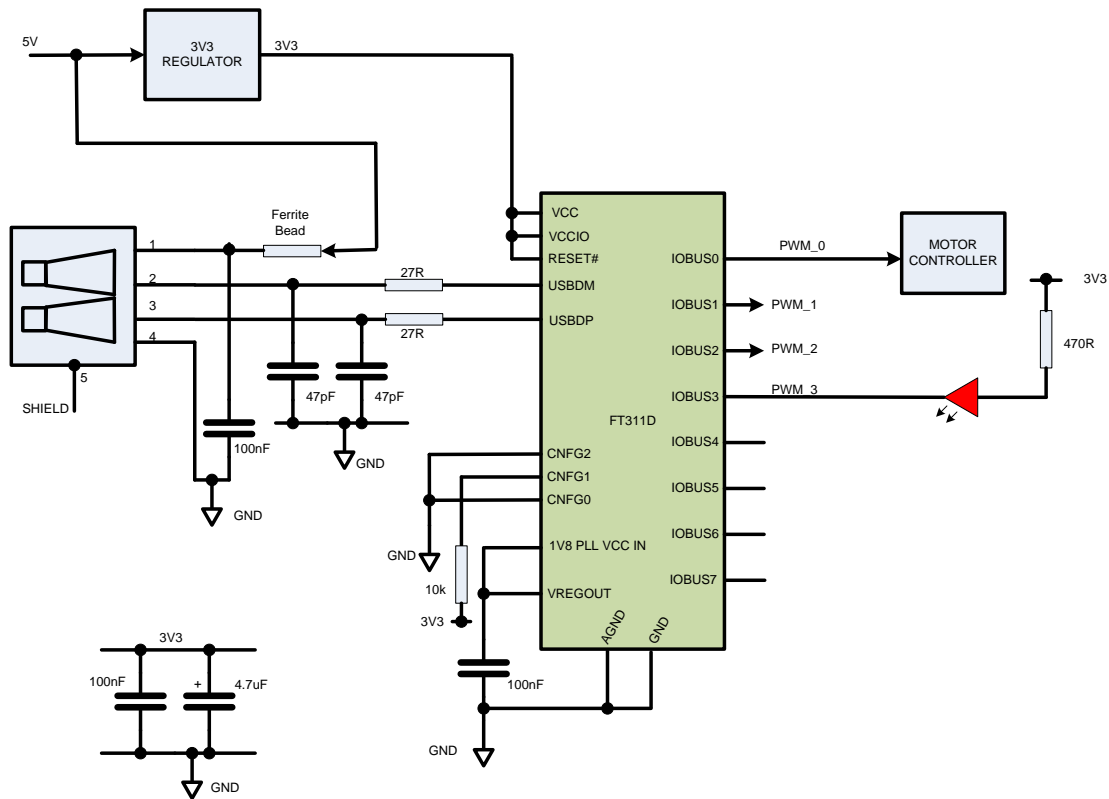


Figure 8.3 Application Example showing USB to PWM Converter

This example shows the CNFGx pins set for mode 010 – Pulse Width Modulation (PWM).

PWM channel 0 has been wired to a motor controller. This is typical of applications with robotic arms or moving machinery.

PWM channel 3 has been connected to an LED. This allows the LED to either flash or by altering the PWM switching frequency the controller can act as a “dimmer switch” to the LED.

The unused channels may be left unterminated.

8.4 USB to I²C (Master) Converter

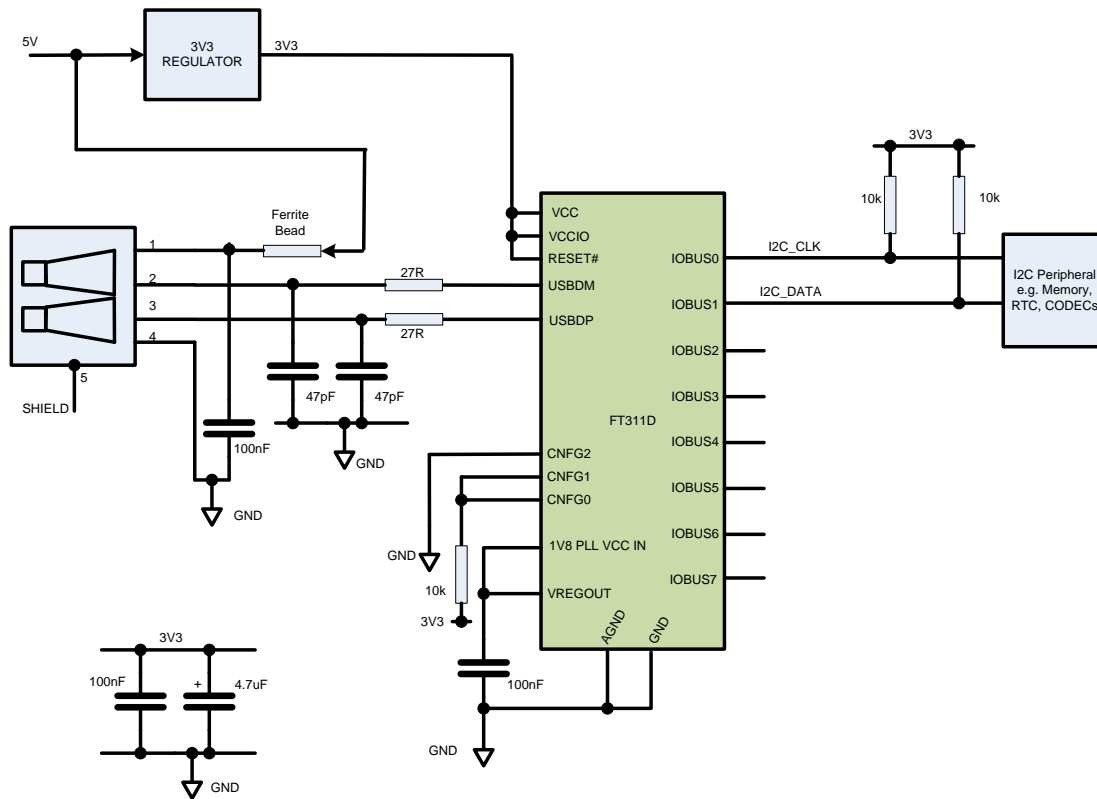


Figure 8.4 Application Example showing USB to I²C (Master) Converter

This example shows the CNFGx pins set for mode 011 – I²C (Master).

Only two signal lines are required for I²C interfacing. The clock is an output from the FT311D while the data line is bi-directional.

Examples of I2C peripherals include EEPROMs, Real time Clocks (RTC) and audio or video codecs.

The unused pins may be left unterminated.

8.5 USB to SPI (Slave) Converter

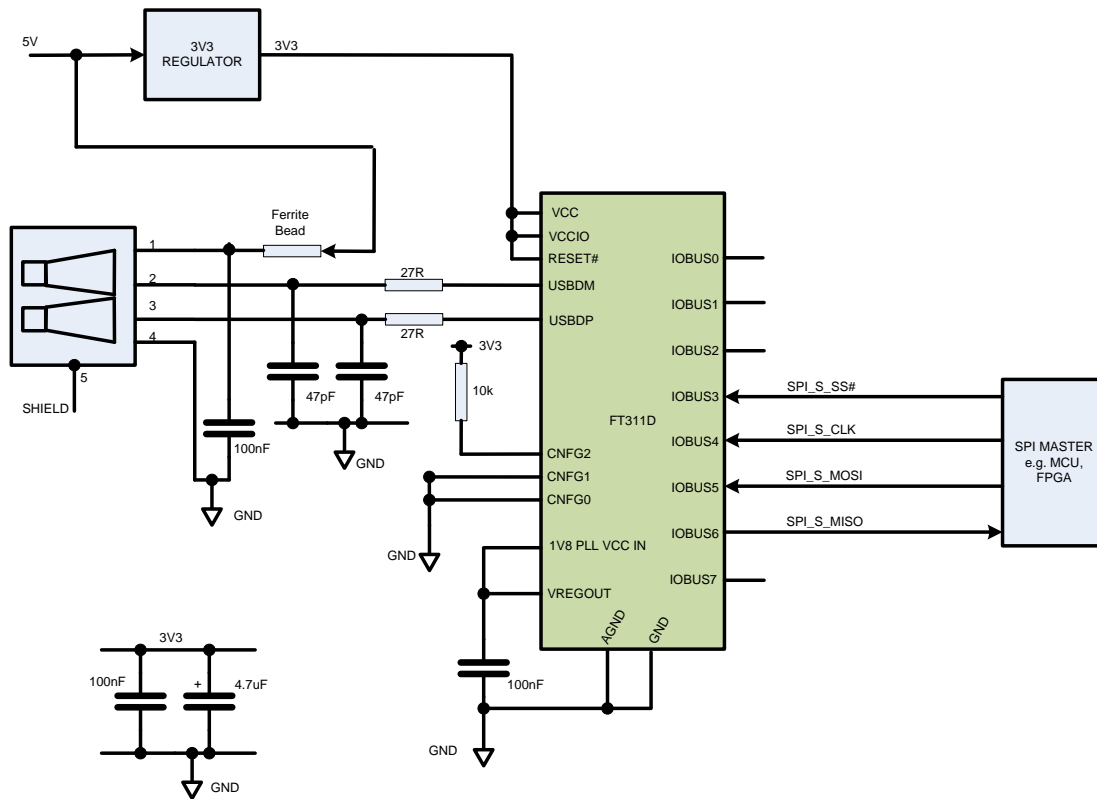


Figure 8.5 Application Example showing USB to SPI (Slave) Converter

This example shows the CNFGx pins set for mode 100 – SPI (Slave).

The external SPI Master controls the slave select line and the clock to the FT311D.

SPI_S_MOSI is the FT311D data input line which may be Most or Least Significant Bit first.

SPI_S_MISO is the FT311D data output line which may be Most or Least Significant Bit first.

Example SPI masters include MCU's and FPGA's

The unused pins may be left unterminated.

8.6 USB to SPI (Master) Converter

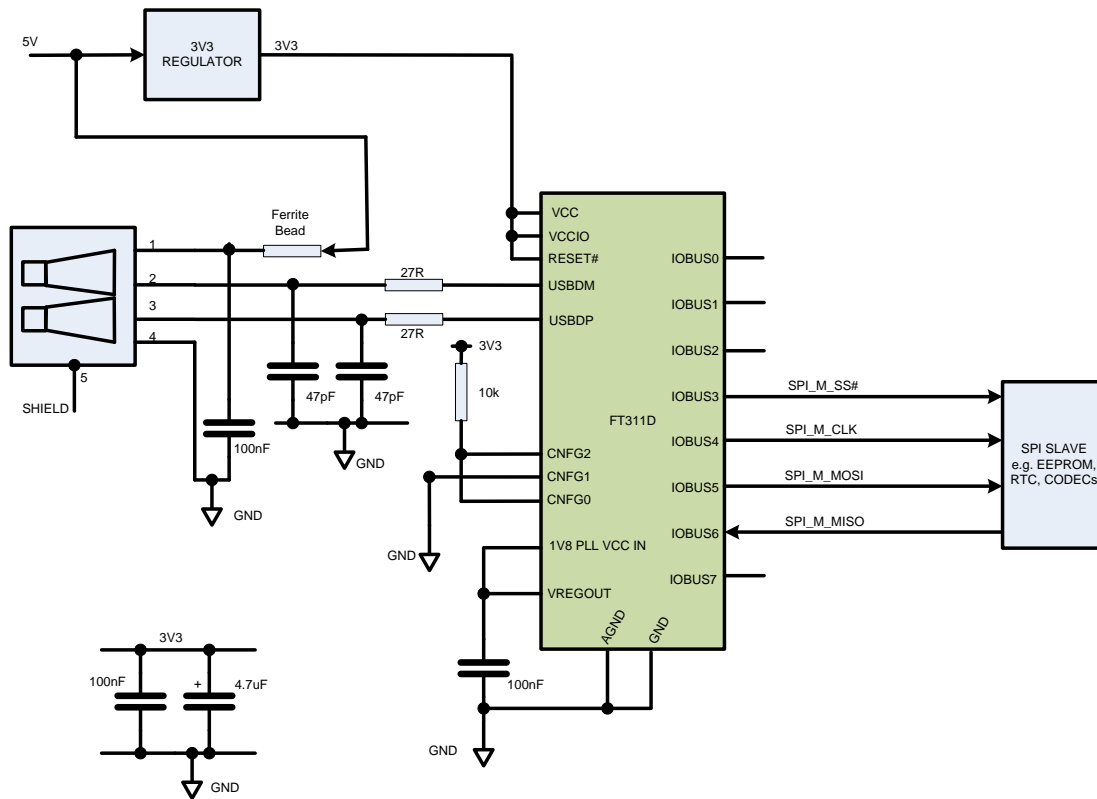


Figure 8.6 Application Example showing USB to SPI (Master) Converter

This example shows the CNFGx pins set for mode 101 – SPI (Master).

The FT311D SPI Master controls the slave select line and the clock to the external SPI slave.

SPI_M_MOSI is the FT311D data output line which may be Most or Least Significant Bit first.

SPI_M_MISO is the FT311D data input line which may be Most or Least Significant Bit first.

Example SPI Slave devices include memory, RTC, and codec devices.

The unused pins may be left unterminated.

9 Package Parameters

FT311D is available in RoHS Compliant packages, QFN package (32QFN) and an LQFP package (32LQFP). The packages are lead (Pb) free and use a 'green' compound. The package is fully compliant with European Union directive 2002/95/EC.

The mechanical drawings of the packages are shown in **sections 9.2**- all dimensions are in millimetres.

The solder reflow profile for all packages can be viewed in **Section 9.3**.

9.1 FT311D Package Markings

9.1.1 QFN-32

An example of the markings on the QFN package are shown in Figure 9-1. The FTDI part number is too long for the 32 QFN package so in this case the last two digits are wrapped down onto the date code line.

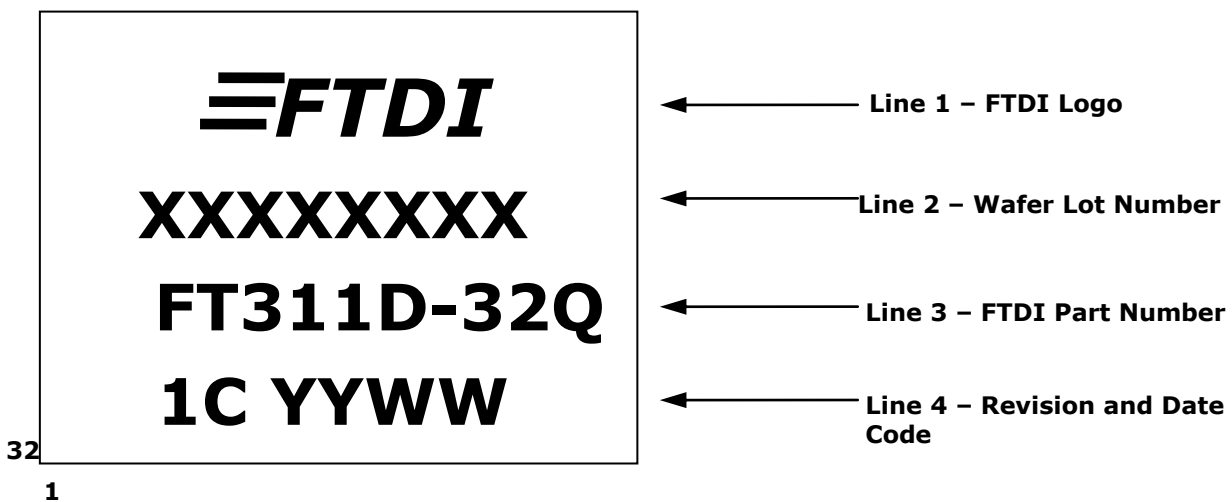


Figure 9-1 QFN Package Markings

1C should be printed on line 4, then a space and then the Date Code.

1. YYWW = Date Code, where YY is year and WW is week number
2. Marking alignment should be centre justified
3. Laser Marking should be used
4. All marking dimensions should be marked proportionally. Marking font should be using Unisem standard font (Roman Simplex)

9.1.2 LQFP-32

An example of the markings on the LQFP package are shown in Figure 9-2.

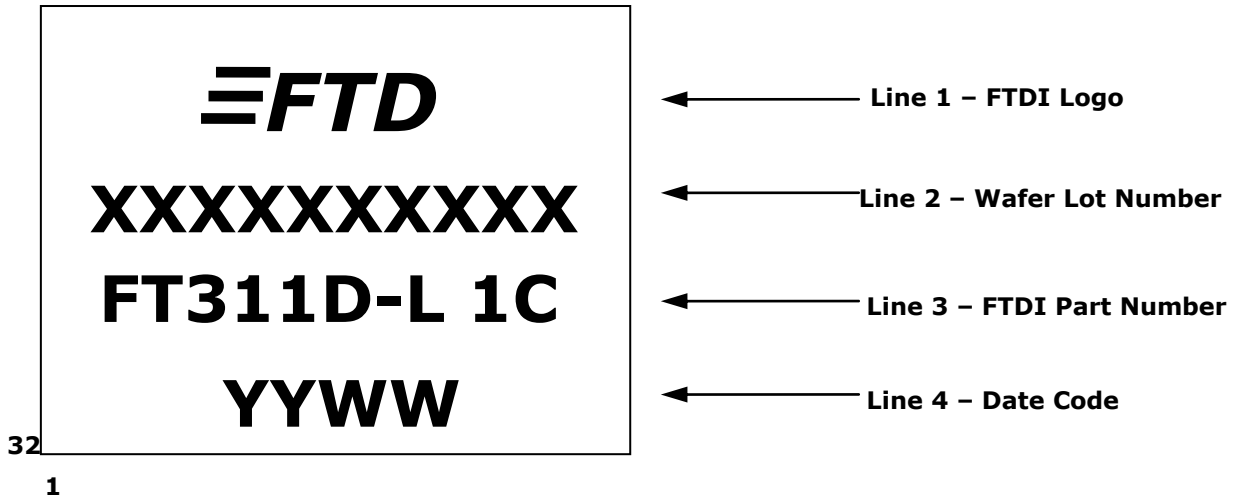


Figure 9-2 LQFP Package Markings

Notes:

1. YYWW = Date Code, where YY is year and WW is week number
2. Marking alignment should be centre justified
3. Laser Marking should be used
4. All marking dimensions should be marked proportionally. Marking font should be using Unisem standard font (Roman Simplex)

9.2 FT311D Package Dimensions

9.2.1 QFN-32 Package Dimensions

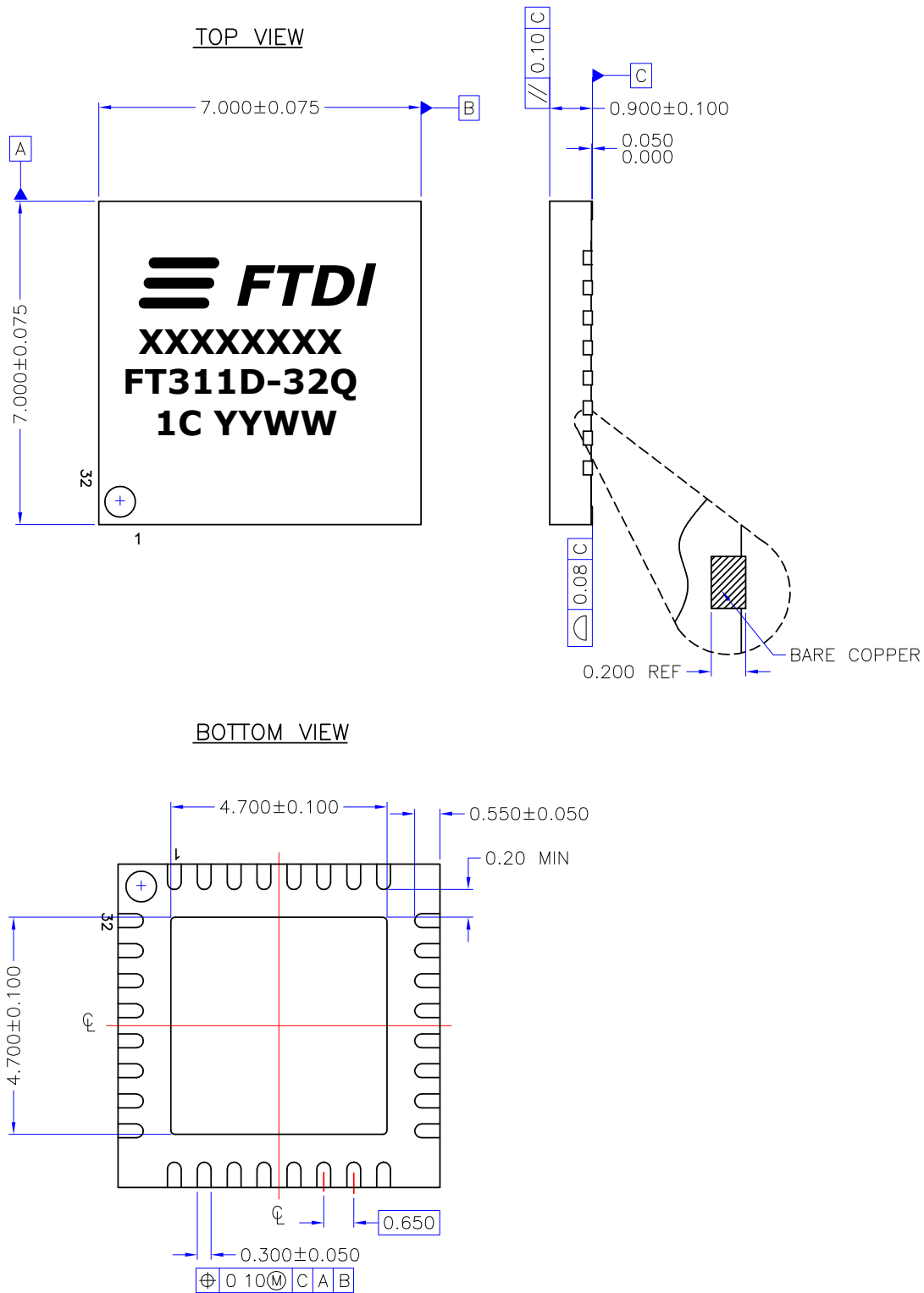


Figure 9-3 QFN-32 Package Dimensions

Note: Dimensions are in mm

Note: The centre pad should be connected to the GND plane for improved thermal conduction and noise immunity.

9.2.2 LQFP-32 Package Dimensions

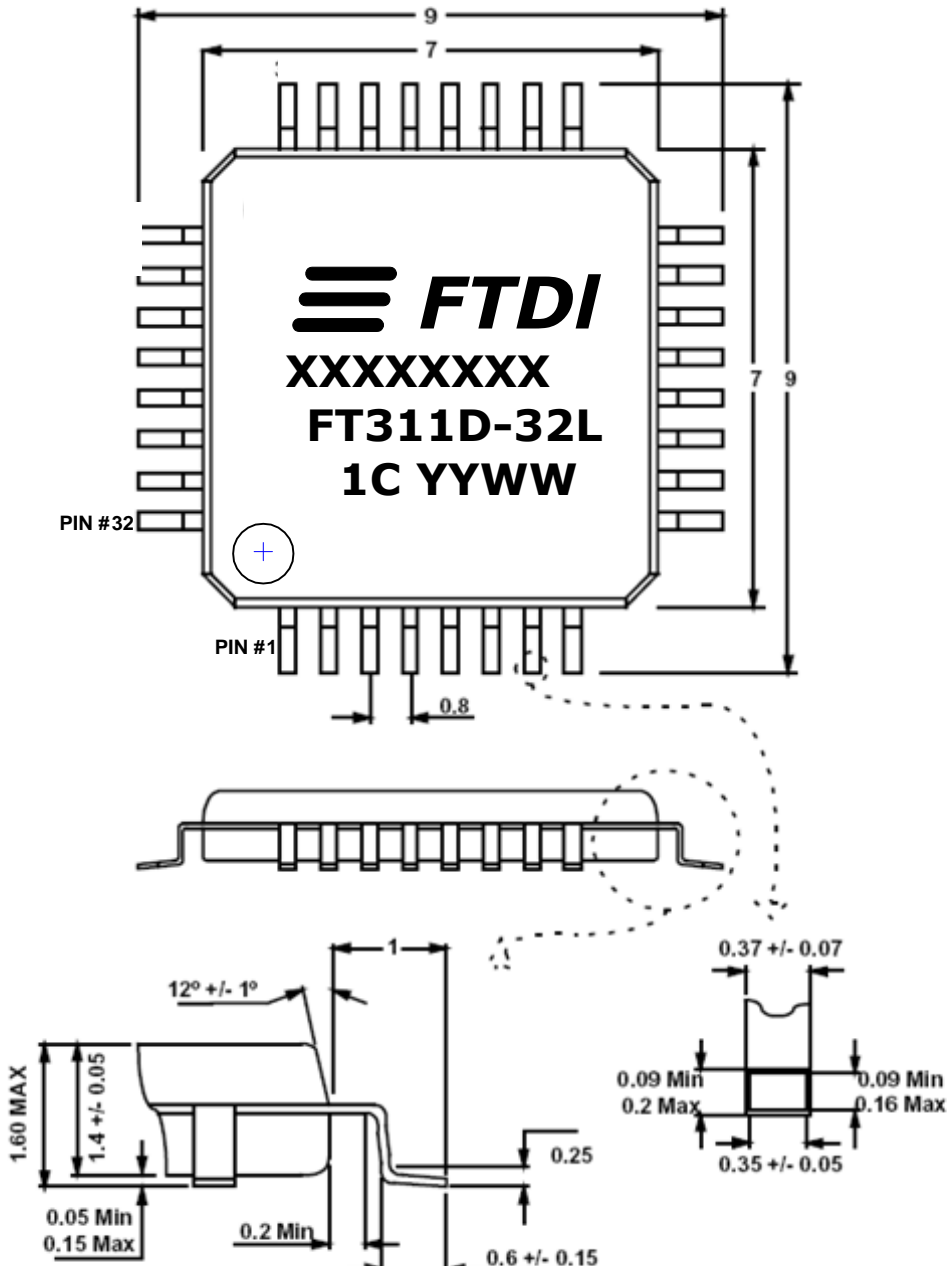


Figure 9-4 LQFP-32 Package Dimensions

Note: Dimensions are in mm

9.3 Solder Reflow Profile

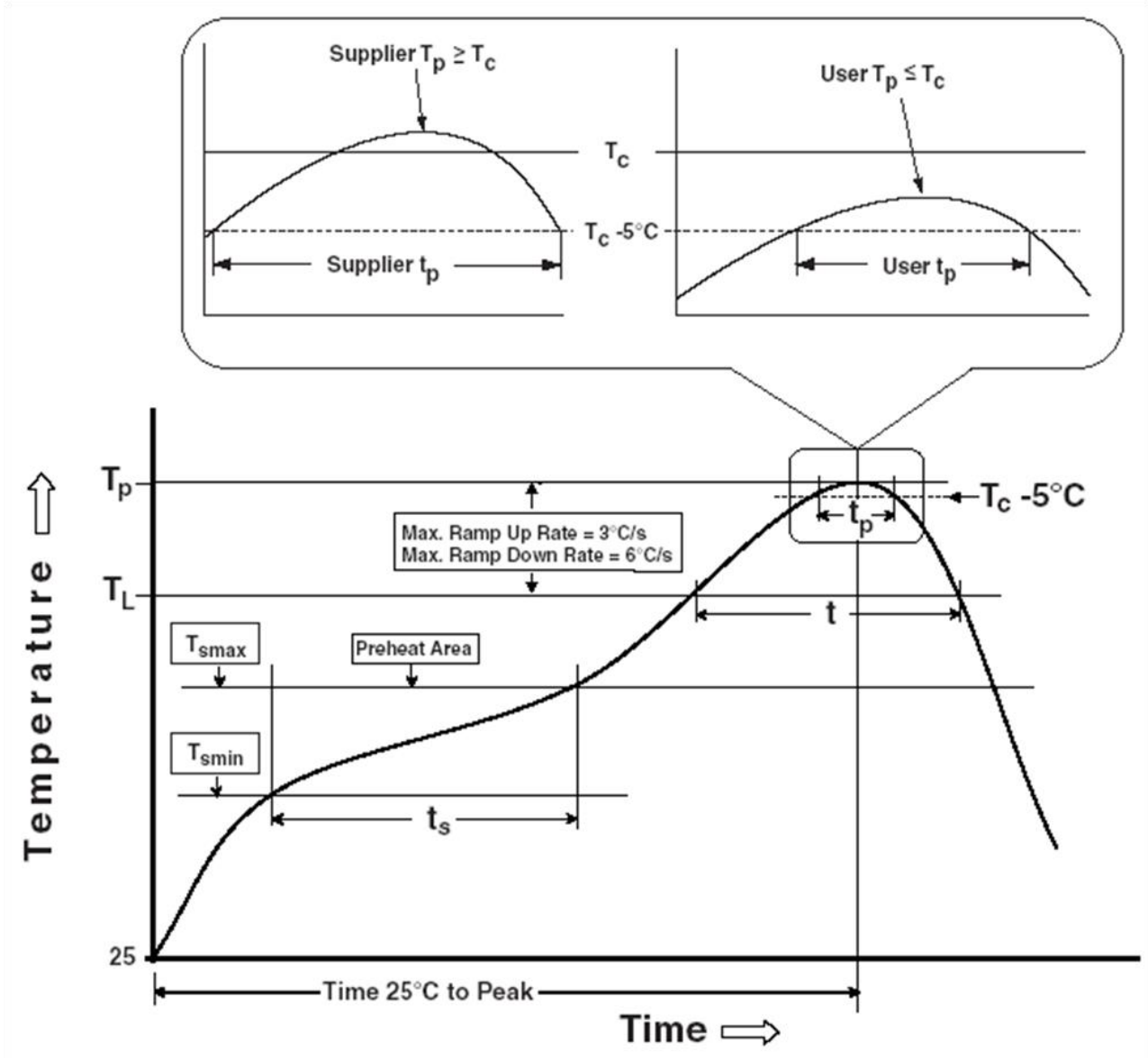


Figure 9-5 All packages Reflow Solder Profile

| Profile Feature | Pb Free Solder Process (green material) | SnPb Eutectic and Pb free (non green material) Solder Process |
|---|--|---|
| Average Ramp Up Rate (T_s to T_p) | 3°C / second Max. | 3°C / Second Max. |
| Preheat - Temperature Min (T_s Min.) - Temperature Max (T_s Max.) - Time (t_s Min to t_s Max) | 150°C 200°C 60 to 120 seconds | 100°C 150°C 60 to 120 seconds |
| Time Maintained Above Critical Temperature T_L : - Temperature (T_L) - Time (t_L) | 217°C 60 to 150 seconds | 183°C 60 to 150 seconds |
| Peak Temperature (T_p) | 260°C | see Figure 9-5 |
| Time within 5°C of actual Peak Temperature (t_p) | 30 to 40 seconds | 20 to 40 seconds |
| Ramp Down Rate | 6°C / second Max. | 6°C / second Max. |
| Time for $T = 25^\circ\text{C}$ to Peak Temperature, T_p | 8 minutes Max. | 6 minutes Max. |

Table 9.1 Reflow Profile Parameter Values

| SnPb Eutectic and Pb free (non green material) | | |
|---|------------------------------|------------------------------|
| Package Thickness | Volume mm ³ < 350 | Volume mm ³ >=350 |
| < 2.5 mm | 235 +5/-0 deg C | 220 +5/-0 deg C |
| ≥ 2.5 mm | 220 +5/-0 deg C | 220 +5/-0 deg C |
| Pb Free (green material) = 260 +5/-0 deg C | | |

Table 9.2 Package Reflow Peak Temperature

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Appendix A – References

Useful Application Notes

http://www.ftdichip.com/Documents/White_Papers/WP_001_Connecting_Peripherals_to_an_Android_Platform.pdf

[http://www.ftdichip.com/Support/Documents/ProgramGuides/FT31XD_Android_programmer_guide\(FT_000532\).pdf](http://www.ftdichip.com/Support/Documents/ProgramGuides/FT31XD_Android_programmer_guide(FT_000532).pdf)

Useful utilities and examples firmware

http://www.ftdichip.com/Support/SoftwareExamples/Android/FT311Configuration_V010100.zip

<http://www.ftdichip.com/Android/SampleApps.zip>

Appendix B - List of Figures and Tables

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Appendix C - Revision History

Document Title: USB Android Host IC FT311D
Document Reference No.: FT_000660
Clearance No.: FTDI# 305
Product Page: <http://www.ftdichip.com/FTProducts.htm>
Document Feedback: [Send Feedback](#)

| | | |
|--------------------|---|---------------|
| Version 1.0 | Initial Release | July 2012 |
| Version 1.1 | VBUSCTRL# pin removed from Figs 8.1 to 8.6 | June 2013 |
| Version 1.2 | Note added for UART and SPI slave enumeration | November 2013 |