# Application Note

# AN_206

# FT1248 1-BIT SPI

**Version 1.0**

**Issue Date:  2012-02-09**

FT1248 is a proprietary FTDI interface that allows for a synchronous parallel/serial interface where the data bus may be 1, 2, 4 or 8 bit wide. This application note describes how the interface may be used with an SPI master in 1-bit data mode.

# Table of Contents

# 1  Introduction

FT1248 is a proprietary FTDI interface currently available in FT220X, FT221X and FT232H devices, that allows for a synchronous parallel/serial interface where the data bus may be 1, 2, 4 or 8 bit wide. This application note describes how the interface may be used with an SPI (Serial Peripheral Interface) master in 1-bit data mode.

## 1.1 Overview

SPI is a recognized industry standard interface for connecting devices in an electronic system. The interface operates on a slave / host basis where one host can access many slaves by addressing each device on the bus with a chip select signal. Data is sent and received synchronously with a clock signal provided by the SPI host. Typically an SPI system will use separate data lines for input and output, but some hosts have a bi-directional data line which would be compatible with the FT1248 1-bit interface.

# 2 Example Circuit

The diagram below shows how the FT220X device could be used as an SPI slave in the 1-bit data configuration.
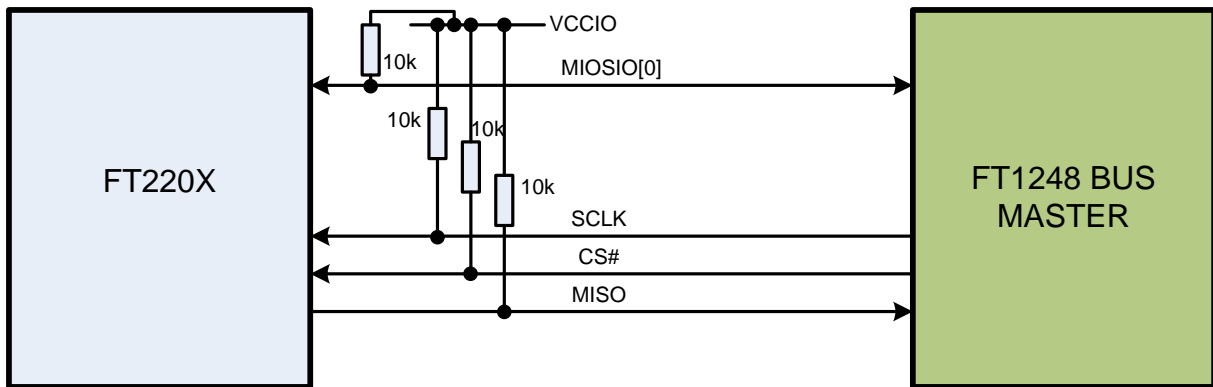


**Figure 2.1 FT220X Configured for 1-bit Data**

The FT220X is the slave device and the external FPGA/MCU is the bus master. The FT220X will auto detect the bus width from the initial command byte sent by the bus master. The other MIOSIO[x] data lines that are not required on the FT220X may be left un-terminated as an internal pull-up ensures the device detects a logic 1.

MIOSIO[0] is the bi-directional data line, which the master must read or write to.

SCLK is the clock from the master to the FT220X. This may be up to 1MHz.

CS# is the active low chip select to enable the FT220X FT1248 interface.

MISO is an output from the FT220X that should be read to obtain the status from the FT1248 interface. The status advices the bus master if the device can accept more data or if data is available to be read.

# 3  FT1248 Interface Description.

FT1248 1-bit mode it requires 8 clock cycles to get 8 data bits and in and 8 clock cycles to get 8 data bits out. Although requiring extra clock cycles compared to using the interface in 8-bit mode it is the most efficient in terms of pin count, required to connect it to the host.

 In the FT1248 there are 3 distinct phases:

While CS# is inactive, the FT1248 reflects the status of the write buffer and read buffers within the FT220X/FT221X on the MIOSIO[0] and MISO wires respectively. The buffers are 512 Bytes each and the status will reflect if at least one byte of space is available for the external device to write to and whether at least one byte is available to be read by the external device.

Additionally, the FT1248 slave supports multiple slave devices where a master can communicate with multiple SPI slave devices. When the slave is sharing buses with other SPI slave devices, the write and read buffer status cannot be reflected on the MIOSIO[0] and MISO wires during CS# inactivity as this would cause bus contention. Therefore, it is possible for the user to select whether they wish to have the buffer status switched on or off during inactivity.

(This setting may be applied in the internal MTP memory with FT_PROG).

When CS#  is active a command/bus size phase occurs first. Following the command phase is the data phase, for each data byte transferred the FT1248 slave drives an ACK/NAK status onto the MISO wire. The master can send multiple data bytes so long as CS# is active, if an unsuccessful data transfer occurs, i.e. a NAK happens on the MISO wire then the master should immediately abort the transfer by de-asserting CS#.
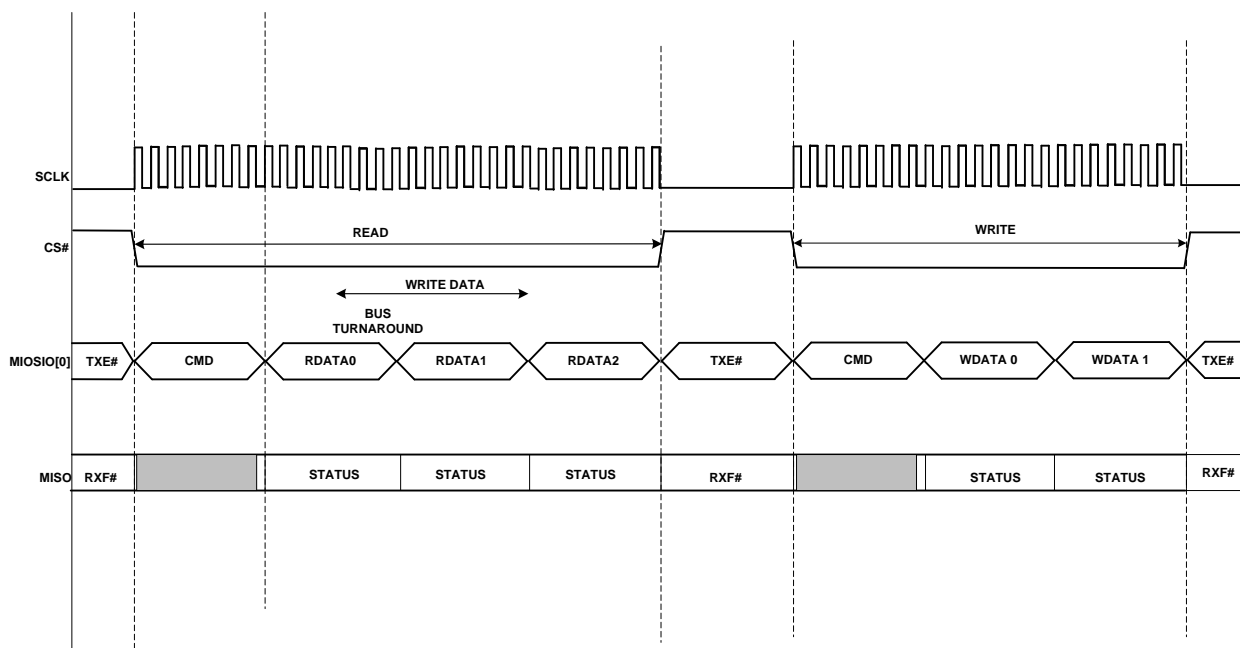


**Figure 3.1: FT1248 Basic Waveform Protocol.**

4

# 3.1 Determining the Dynamic Bus Width

The bus width is dynamic. In order for the FT220X/FT221X, in FT1248 mode, to determine the bus width within the command phase, the bus width is encoded along with the actual commands on the first active clock edge when CS# is active and has a data width of 4-bits.

If any of the MIOSIO[3:2] signals are driven low by the external host then the data transfer width equals 4-bits

If MIOSIO[1] signal is driven low by the external host then the data transfer width equals 2-bits

Else the bus width is defaulted to 1-bit

In order to successfully decode the bus width, all MIOSIO signals must have pull up resistors. By default, all MIOSIO signals shall be seen by the FT220X/FT221X in FT1248 mode as logic '1'from the internal resistors. This means that when a FT1248 master does not wish to use certain MIOSIO signals, the slave (FT220X / FT221X) is still capable of determining the requested bus width since any unused MIOSIO signals shall be pulled up by default.

The remaining bits used during the command phase are used to contain the command itself which means that it is possible to define up to 16 unique commands.

|  | LSB | | | | | | | MSB |
|---|---|---|---|---|---|---|---|---|
|  | CMD[3] | BWID 2-bit | BWID 4-bit | CMD[2] | BWID 8-bit | CMD[1] | CMD[0] | X |
|  | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 1-bit Bus Width | CMD[3] | X | X | CMD[2] | X | CMD[1] | CMD[0] | X |
|  | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 2-bit Bus Width | CMD[3] | 0 | X | CMD[2] | X | CMD[1] | CMD[0] | X |
|  | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 4-bit Bus Width | CMD[3] | X | 0 | CMD[2] | X | CMD[1] | CMD[0] | X |
|  | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |

Figure 3.2: FT1248 Command Structure

## 3.2 Supported Commands on the FT1248 Interface

The FT1248 interface can accept and decode up to 16 unique commands. At this time only 9 unique commands are implemented as shown below.

| Command | Identifier | Description |
|---|---|---|
| write | 0x00 | Write request command |
| read | 0x01 | Read request command |
| read modem status | 0x02 | Read modem status command, users may wish to emulate modem status control. A RMS command returns status bits RTS and DTR |
| write modem status | 0x03 | Write modem status command, users may wish to emulate modem status control. A WMS command allows users to set status bits: DCD, RI, DSR, CTS |
| write buffer flush | 0x04 | Write buffer flush request – This command is used to indicate to the FT1248 slave that its write buffers should be flushed rather than wait for any latency timers to expire. If this command is received the FT1248 block will flag the upstream controllers (USB FIFOs etc) to flush their write buffers regardless of what content is present in the FT1248 write buffer |
| address eeprom | 0x05 | Address EEPROM command sets the address users wish to write or read from |
| write eeprom | 0x06 | Write EEPROM command sets the write data to be written into the EEPROM |
| read eeprom | 0x07 | Read EEPROM command reads |
| read usb status | 0x08 | Read USB Status:  00 = suspended, 01 = default, 10 = addressed, 11 = configured |
| Reserved | 0x09 – 0xF | Unused Commands |

**Table 3.1: FT1248 Commands**

## 3.3 LSB or MSB Selection

The data can be sent/received Least Significant Bit First (LSB) or Most Significant Bit First (MSB). To determine which mode is used by the FT1248 interface of the FT220X the MTP memory must be set.

This may be selected with FT_PROG.

## 3.4 Clock Phase/Polarity

The FT1248 slave does not need to have any knowledge of clock rate as this is supplied by the FT1248 master. However the relationship between clock and data needs to be controllable, to allow the slave to operate in the same way as the master such that data is correctly driven and sampled on the correct clock phases. By configuring the polarity and phase of CLK with respect to the data it is possible to match the FT1248 (SPI) master.

There are 4 possible modes which are determined by the Clock Polarity (CPOL) and Clock Phase (CPHA) signals. The different combinations of these signals are commonly referred to as modes, see Table 3.2 below. For the FT1248 slave, only 2 of these 4 modes are supported. CPHA will always be set to 1 in the FT1248 slave because data is available or driven on to MIOSIO wires on the first clock edge after CS# is active and is therefore sampled on the trailing edge of the first clock pulse. When CPHA equals 0, it means data must be available or driven onto the MIOSIO wires on the first leading edge of the clock after CS# is active. However, during this period between CS# becoming active and the first leading clock edge is when the MIOSIO wires are being "turned around" as when CS# is inactive the FT1248 slave is driving the write buffer status. Supporting CPHA = 0 would result in bus contention and therefore, shall not be supported.

| Mode | CPOL | CPHA | Supported |
|---|---|---|---|
| 0 | 0 | 0 | NO |
| 1 | 0 | 1 | YES |
| 2 | 1 | 0 | NO |
| 3 | 1 | 1 | YES |

**Table 3.2: CPOL & CPHA Mode Numbers**

When CPOL is 1, the idle state of the clock is high. When CPOL is 0, the idle state of the clock is low. It should be noted that clock phase and polarity need to be identical for the master and attached slave device.

### 3.4.1  CPHA = 1

When CPHA is set to '1', the first edge after CS# goes low will be used to shift (or drive) the first data bit onto MIOSIO. Every odd numbered edge after this will shift out the next data bit. Incoming data will be sampled on the second or trailing SCLK edge and every even edge thereafter.

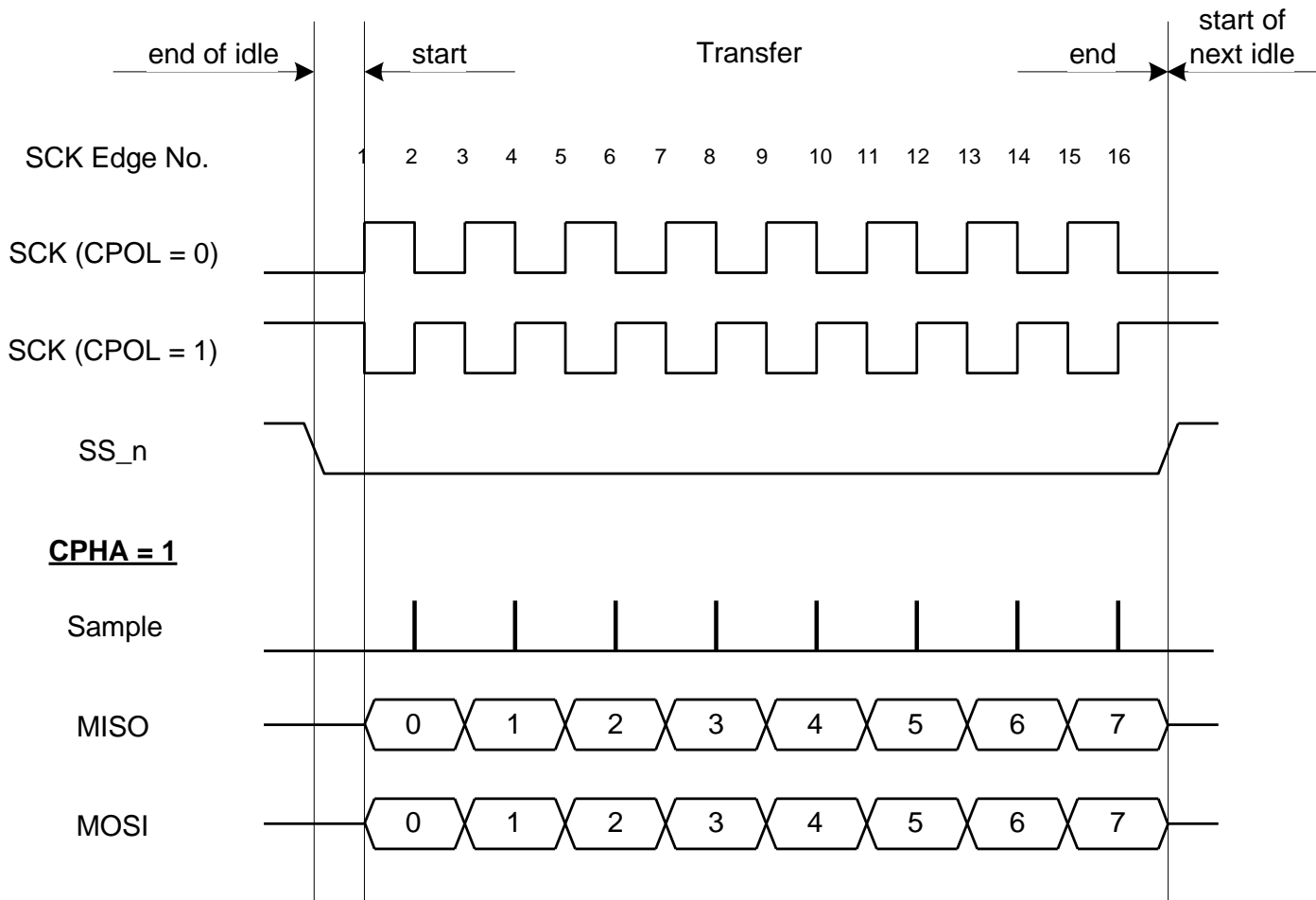Figure 3.3 shows this for both CPOL = 0 and CPOL = 1.

**Figure 3.3: FT1248 Clock Format CPHA = 1**

Note:   The CPOL value may be selected in the MTP memory. This may be done with FT_PROG.

Note:   Further information on this interface can be found in AN_167_FT1248 Parallel Serial
Interface Basics from the FTDI website www.ftdichip.com.
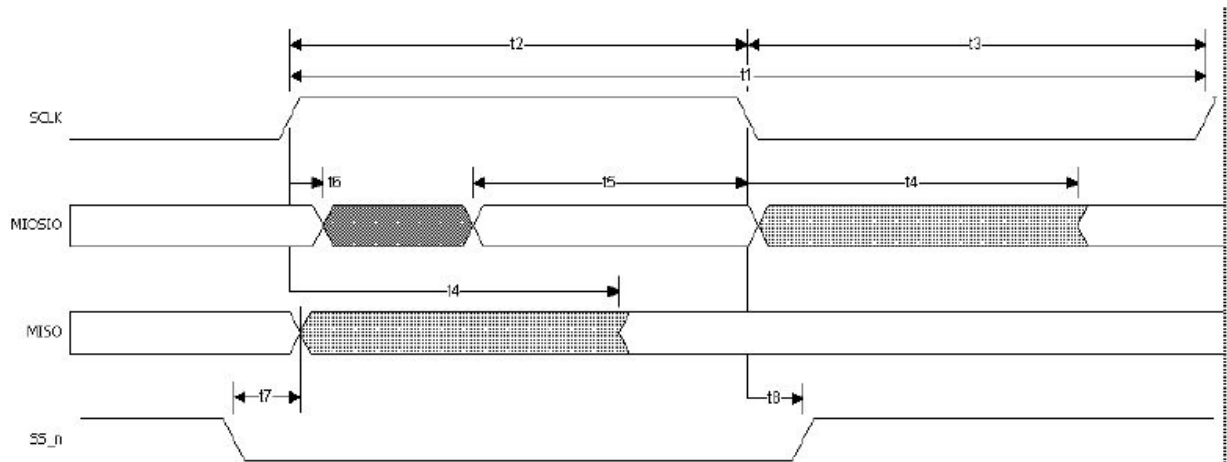
## 3.5 FT1248 Timing



**Figure 3.4: FT1248 Clock Format CPHA = 1**

The timings will vary depending on VCCIO.

|    | Min (ns) | Typical (ns) | Max (ns) | Description |
|----|----------|--------------|----------|-------------|
| T1 |          | 83.33ns      |          | SCLK Period |
| T2 |          | 41.67ns      |          | SCLK HIGH |
| T3 |          | 41.67ns      |          | SCLK LOW |
| T4 |          | 1            | 30       | SCLK rising or falling driving edge to MIOSIO/MSIO |
| T5 |          | 25           |          | MIOSIO setup time to rising or falling sample SCLK edge |
| T6 |          | 3            |          | MIOSIO hold time from rising or falling sample SCLK edge |
| T7 |          | 5            |          | SS_n setup time to rising or falling SCLK edge |
| T8 |          | 5            |          | SS_n hold time from rising or falling sample SCLK edge |

**Table 3.3: 1V8 VCCIO timings**

|  | Min (ns) | Typical (ns) | Max (ns) | Description |
|---|---|---|---|---|
| T1 |  | 83.33ns |  | SCLK Period |
| T2 |  | 41.67ns |  | SCLK HIGH |
| T3 |  | 41.67ns |  | SCLK LOW |
| T4 |  | 1 | 15 | SCLK rising or falling driving edge to MIOSIO/MSIO |
| T5 |  | 22 |  | MIOSIO setup time to rising or falling sample SCLK edge |
| T6 |  | 1 |  | MIOSIO hold time from rising or falling sample SCLK edge |
| T7 |  | 5 |  | SS_n setup time to rising or falling SCLK edge |
| T8 |  | 5 |  | SS_n hold time from rising or falling sample SCLK edge |

**Table 3.4: 2V5 VCCIO timings**

|  | Min (ns) | Typical (ns) | Max (ns) | Description |
|---|---|---|---|---|
| T1 |  | 83.33ns |  | SCLK Period |
| T2 |  | 41.67ns |  | SCLK HIGH |
| T3 |  | 41.67ns |  | SCLK LOW |
| T4 |  | 1 | 10 | SCLK rising or falling driving edge to MIOSIO/MSIO |
| T5 |  | 20 |  | MIOSIO setup time to rising or falling sample SCLK edge |
| T6 |  | 0 |  | MIOSIO hold time from rising or falling sample SCLK edge |
| T7 |  | 5 |  | SS_n setup time to rising or falling SCLK edge |
| T8 |  | 5 |  | SS_n hold time from rising or falling sample SCLK edge |

**Table 3.5: 3V3 VCCIO timings**

# 4  Contact Information

**Head Office – Glasgow, UK**

Future Technology Devices International Limited
Unit 1, 2 Seaward Place, Centurion Business Park
Glasgow G41 1HH
United Kingdom
Tel: +44 (0) 141 429 2777
Fax: +44 (0) 141 429 2758

E-mail (Sales)                sales1@ftdichip.com
E-mail (Support)            support1@ftdichip.com
E-mail (General Enquiries)  admin1@ftdichip.com

**Branch Office – Hillsboro, Oregon, USA**

Future Technology Devices International Limited
(USA)
7235 NW Evergreen Parkway, Suite 600
Hillsboro, OR 97123-5803
USA
Tel: +1 (503) 547 0988
Fax: +1 (503) 547 0987

E-Mail (Sales)              us.sales@ftdichip.com
E-Mail (Support)           us.support@ftdichip.com
E-Mail (General Enquiries) us.admin@ftdichip.com

**Branch Office – Taipei, Taiwan**

Future Technology Devices International Limited
(Taiwan)
2F, No. 516, Sec. 1, NeiHu Road
Taipei 114
Taiwan , R.O.C.
Tel: +886 (0) 2 8791 3570
Fax: +886 (0) 2 8791 3576

E-mail (Sales)                tw.sales1@ftdichip.com
E-mail (Support)            tw.support1@ftdichip.com
E-mail (General Enquiries)  tw.admin1@ftdichip.com

**Branch Office – Shanghai, China**

Future Technology Devices International Limited
(China)
Room 408,  317 Xianxia Road,
Shanghai, 200051
China
Tel: +86 21 62351596
Fax: +86 21 62351595

E-mail (Sales)              cn.sales@ftdichip.com
E-mail (Support)           cn.support@ftdichip.com
E-mail (General Enquiries) cn.admin@ftdichip.com

**Web Site**

http://ftdichip.com

# Appendix A – References

## Document References

[FT232H Data Sheet](#)

[FT220X Data Sheet](#)

[FT221X Data Sheet](#)


[AN_167_FT1248_Parallel_Serial_Interface_Basics](#)

## Acronyms and Abbreviations

| Terms | Description |
|-------|-------------|
| SPI | Serial Peripheral Interface |
| USB | Universal Serial Bus |
| USB-IF | USB Implementers Forum |
|  |  |
|  |  |

NOTE – put terms in alphabetical order.

# Appendix B – List of Tables & Figures

## List of Tables

## List of Figures

# Appendix C – Revision History

Document Title:             AN_206 FT1248 1-BIT SPI

Document Reference No.:     FT_000625

Clearance No.:              FTDI# 276

Product Page:               http://www.ftdichip.com/FT-X.htm

Document Feedback:          Send Feedback

| Revision | Changes | Date |
|----------|---------|------|
| 1.0 | Initial Release | 2012-02-09 |
| | | |
| | | |
| | | |
| | | |
| | | |