Technical Note

TN_168

FT600_601 Errata Technical Note

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The intention of this errata technical note is to give a detailed description of known functional or electrical issues with the FTDI FT600/FT601 devices.

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1 Glossary of Terms

Sl.No.	Term	Description
1	Aligned write	An aligned write is a write on the FIFO interface with all byte enables selected, i.e. on a 16-bit interface, an aligned write is 16-bits wide and on a 32-bit interface, an aligned write is 32-bits wide.
2	Unaligned write	An unaligned write is a write on the FIFO interface that is not as wide as the interface, i.e. on a 16-bit interface, an unaligned write is a single byte write and on a 32-bit interface, an unaligned write is 1, 2, or 3 bytes.
3	Aligned read	An aligned read is a read from the FIFO interface when the slave asserts all byte enables. On a 16-bit interface, an aligned read is 16-bits wide and on a 32-bit interface, an aligned read is 32-bits wide
4	Unaligned read	An unaligned read is a read from the FIFO interface that is not as wide as the interface, i.e. on a 16-bit interface, an unaligned read is a single byte read and on a 32-bit interface, an unaligned read is 1, 2, or 3 bytes. An unaligned read from the slave always signals that it is a short packet
5	ZLP	A USB Zero-length packet
6	Short packet	A short packet – a packet that is less than the full packet size. In USB2.0 (High Speed), a short packet has a non-zero length less than 512 bytes and in USB 3.0 (Super Speed), a short packet has a non-zero length less than 1024 bytes. Short packet signals an end of transfer on the endpoint.
7	Full packet	In USB2.0 (High Speed), a full packet has a length equal to 512 bytes and in USB 3.0 (Super Speed); a full packet has a length equal to 1024 bytes.
8	Session	A session consists of one or more USB transfers. A session is created when a read or write request is received by the driver layer. A session ends when the required length of data has been transferred or a short packet is received (session underrun).
9	Session Underrun	A session underrun is detected when a read request is active and the FIFO interface master wrote less than the requested number of bytes and stopped. e.g. If 1MB of data is requested in a read request, and the FIFO interface master wrote only 1025 bytes and stopped, the device detects this condition as a session underrun and ends the session.
10	Cancel Session On Underrun	This option is the default. The device closes a session when it detects an underrun. An underrun is detected when the FIFO interface reports that the master has stopped writing data before the FIFO buffer is full and the session requested length has not been reached.

2 Errata List

2.1 Erratum 0001

Erratum	0001	Additional Notes
Title	A control message in the middle of an internal IN data transfer will cause the transfer to hang	
Severity	High	
Affected Revisions	FT600-Revision A, FT601-Revision A	
Detailed Description	When the device is transferring data from a FIFO buffer to the EPC buffer of an IN endpoint and a control message is received simultaneously, the transfer will not complete and the device remains in this state and becomes unresponsive. The device remains in this state and a subsequent power cycle is required.	
Workaround	There is no workaround for the above problem. Control messages shall not be sent to the device while IN transfers are in progress.	
Fix Status	FT600-Revision B FT601–Revision B	
Fix Description	Control messages shall be queued while data transfer is in progress	

Table 1 - Erratum 001

2.2 Erratum 0002

Erratum	0002	Additional Notes
Title	Detach/attach the device during IN transfers requires a power cycle	
Severity	High	
Affected Revisions	FT600-Revision A FT601-Revision A	
Detailed Description	In self-powered devices, when the device is transferring data from a FIFO buffer to the EPC buffer of an IN endpoint and a USB disconnect event is received simultaneously, the transfer will not complete and the device becomes unresponsive. The device remains in that state and a subsequent power cycle is required.	
Workaround	A device reset circuit upon loss of VBUS may be added to ensure that the device is reset after a detach event.	
Fix Status	FT600-Revision B FT601–Revision B	
Fix Description	The detach event shall be blocked during data transfer to the IN endpoint	

Table 2 - Erratum 0002

2.3 Erratum 0003

Erratum	0003	Additional Notes
Title	A ZLP is not sent to the host when the FIFO interface master writes a multiple of full packets and stops while the FIFO buffer has more space	
Severity	Medium	
Affected Revisions	FT600-Revision A, FT601-Revision A	
Detailed Description	When the 'Cancel Session On Underrun – Disabled' option is not selected, the device closes read sessions when a session underrun is detected. When the FIFO interface master stops a write access after a multiple of full packets has been written continuously, the device transfers the last full packet to the host and closes the transfer without sending a ZLP to end the transfer at the host. The missing ZLP leads to a read timeout at the host.	Example: Buffer = 4kB. Host makes a read request for 12KB to the device. Session is opened at the device and the master begins to write data and stops after 1kB. The device detects this as the master has ended the session. The device transfers the 1kB to the host and ends the session. No ZLP is sent. At the host, the session times out and abort recovery procedures are required.
Workaround	1. Select the 'Cancel Session On Underrun – Disabled' configuration option. When this configuration option is selected, the device keeps the read session open and the master may stop writing at full packet boundaries only and continue. The session is closed in the device and host when one of the following conditions is met: a. master writes a short packet b. the requested read length is reached Any condition other than the above will lead to a read timeout and abort recovery procedures are required. 2. The host application may enable Stream Pipe on the endpoint and set the size to 1KB. At the same time, the host application may issue multiple asynchronous read requests of 1KB. However, this approach will have a performance drawback in terms of CPU MIPs and poor throughput	
Fix Status	FT600-Revision B FT601–Revision B	
Fix Description	A programmable timeout shall be provided to detect that the FPGA master has no more data and a ZLP will be returned to end the transfer and close the session	

Table 3 - Erratum 0003

2.4 Erratum 0004

Erratum	0004	Additional Notes
Title	A ZLP is not sent to the host when the FIFO interface master writes a full packet which fills the FIFO buffer and stops before the requested length of data is transferred	
Severity	Medium	
Affected Revisions	FT600-Revision A FT601-Revision A	
Detailed Description	The device uses a double buffered system to receive data from the FIFO interface master. These buffers are known as FIFO buffers and each buffer can contain a multiple of full packets. When a buffer is completely filled, the device switches to the next buffer to receive more data from the FPGA master. If the master stops writing into the FIFO at the switchover, the device waits indefinitely for more data from the master.	Example: Buffer size = 4kB. The host makes a read request for 12kB to the device. A session is opened at the device and the master begins to write data and stops after 4kB. The 4kB of data is shipped to the host and the device moves to the next 4kB buffer and waits for data. Eventually the host will timeout and abort recovery processing is required
Workaround	Select the 'Cancel Session On Underrun – Disabled' configuration option. When this configuration option is selected, the device keeps the read session open and the master may stop writing at full packet boundaries only and continue, including at buffer switchovers. The session is closed in the device and host when one of the following conditions is met: a. master writes a short packet b. the requested read length is reached Any condition other than the above will lead to a read timeout and abort recovery procedures are required.	
Fix Status	FT600-Revision B FT601–Revision B	
Fix Description	A programmable timeout option shall be provided via the Chip configuration utility to detect that the FIFO interface master has no more data and a ZLP will be returned to end the transfer and close the session	

Table 4 - Erratum 0004

2.5 Erratum 0005

Erratum	0005	Additional Notes
Title	FIFO clock disappears when the device enters suspend	
Severity	Medium	
Affected Revisions	FT600-Revision A, FT601-Revision A	
Detailed Description	When a USB Suspend is signaled, the device enters a low power state and turns off the FIFO clock.	
Workaround	The FIFO interface master shall be designed to handle the interface clock stoppage	
Fix Status	FT600-Revision B FT601–Revision B	
Fix Description	A configuration option shall be provided that may be enabled and disabled. When enabled, then the FIFO clock shall remain enabled during SUSPEND and when disabled, the FIFO clock shall be turned off.	

Table 5 - Erratum 0005

2.6 Erratum 0006

Erratum	0006	Additional Notes
Title	Keep FIFO Clock On In Suspend does not work with USB 2.0	
Severity	Medium	
Affected Revisions	FT600-Revision A, FT601-Revision A, FT600-Revision B FT601–Revision B	
Detailed Description	When "Keep FIFO clock On In Suspend" option is selected and when the device enters suspend mode while the active PHY is USB2.0, then the device becomes unresponsive and a power cycle is required to recover. The consequences of this issue are that the device will not function in a USB2.0 host port and the device is highly likely to fail in a USB3.0 host port. It is highly likely to fail in a USB3.0 host port because a host may switch from USB3.0 to USB2.0 mode during a power-cycle sequence or while exiting from hibernate state followed by a SUSPEND. When the device PHY switches into USB2.0 while the FIFO clock on is active and receives a SUSPEND, the issue will manifest.	The BIOS/UEFI program in a PC, at boot-up or upon exit from hibernate, initializes the USB host as a USB2.0 host. A USB3.0 capable device, connected to such a port, follows suit and enables its USB2.0 PHY. The BIOS/UEFI may continue to enumerate the attached devices and SUSPEND them before passing control to the OS. The OS then RESUMEs the devices, issues a RESET and switches to USB3.0 mode. As the device enters SUSPEND while in USB2.0 mode, it becomes unresponsive if the option is enabled.
Workaround	There is no workaround and the option shall not be selected in the configuration programmer to avoid this issue. If the selection has been previously enabled in the configuration, then the device has to be connected to a USB3.0 host port with a USB3.0 cable and re-configured to disable the option.	
Fix Status	Fix by masking the option in the next version of configuration programmer.	
Fix Description	A new version of configuration programmer shall be released in which this option is removed.	

2.7 Erratum 0007

Erratum	0007	Additional Notes
Title	Disable Chip Power Down does not work with USB2.0	
Severity	Medium	
Affected Revisions	FT600-Revision B FT601–Revision B	
Detailed Description	When "Disable Chip Power Down" option is enabled, the configuration setting internally enables the "Keep FIFO Clock On in suspend". This causes Erratum 0006 to manifest.	
Workaround	There is no workaround and the option shall not be selected in the configuration programmer to avoid this issue. If the selection has been previously enabled in the configuration, then the device has to be connected to a USB3.0 host port with a USB3.0 cable and re-configured to disable the option.	
Fix Status	Fix by masking the option in the next version of configuration programmer.	
Fix Description	A new version of configuration programmer shall be released in which this option is removed.	

3 Contact Information

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Distributor and Sales Representatives

Please visit the Sales Network page of the FTDI Web site for the contact details of our distributor(s) and sales representative(s) in your country.

Appendix A – References

Document References

NA

Acronyms and Abbreviations

Terms	Description
EPC	Embedded Packet Capture
FIFO	First In First Out
FPGA	Field Programmable Gate Array
USB	Universal Serial Bus
VBUS	USB Voltage Supply (nominal: +5V)
ZLP	Zero Length Packet

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Appendix C – Revision History

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1.0	Initial Release	2016-07-07
1.1	Added Erratum 0006 & 0007	2017-05-08